Agilent ParBERT 81250

Parallel Bit Error Ratio Tester

Product Overview

Version 5.1 (Corresponds to ParBERT 81250 Software revision 5.1)

The Only Parallel Bit Error Ratio Solution for testing at 675 Mbit/s, 1.65 Gbit/s, 2.7 Gbit/s, 3.35 Gbit/s, 10.8 Gbit/s, 13.5 Gbit/s and 45 Gbit/s

Agilent Technologies

Agilent ParBERT 81250

Agilent ParBERT 81250 is a modular parallel electrical and optical bit error ratio (BER) test platform, which works up to 45 Gbit/s. The ParBERT 81250 platform comprises modules that work at 675 Mbit/s, 1.65 Gbit/s, 2.7 Gbit/s, 3.35 Gbit/s, 10.8 Gbit/s and 45 Gbit/s. The system generates pseudo random word sequences (PRWS), standard pseudo random binary sequences (PRBS) and user-defined patterns on parallel lines. You can analyze bit error ratios with user-defined patterns, PRBS/PRWS or mixed data (a combination of user-defined patterns and PRBS).

ParBERT 81250 is a perfect fit for parallel-to-serial, serial-to-parallel, serial-to-serial and multiple serial BER test. Examples comprise multiplexer and demultiplexer (Mux/Demux) - or SerDes (serializer/deserializer) - testing used in telecom and storage area network (SAN) ICs, multiple transmitter and receiver testing in manufacturing, amplifiers as well as 10GbE and forward error correction (FEC) device testing.

ParBERT 81250 also provides data and control signals for the DUT if required.

The ParBERT Software Suite is a ready-to-use package, which offers different levels of measurement analysis:

1. Fast pass/fail measurements ideal for production
2. Output Timing measurements provide results for setup & hold times, skew between channels, phase margins, detailed Jitter results (RJ/DJ/TJ), and eye opening specification results
3. Output level measurements provide results for high/low levels, amplitudes, threshold margins and Q-factor analysis
4. Graphical results for detailed root cause analysis - see trends clearly and fast, e.g. color and contour plots

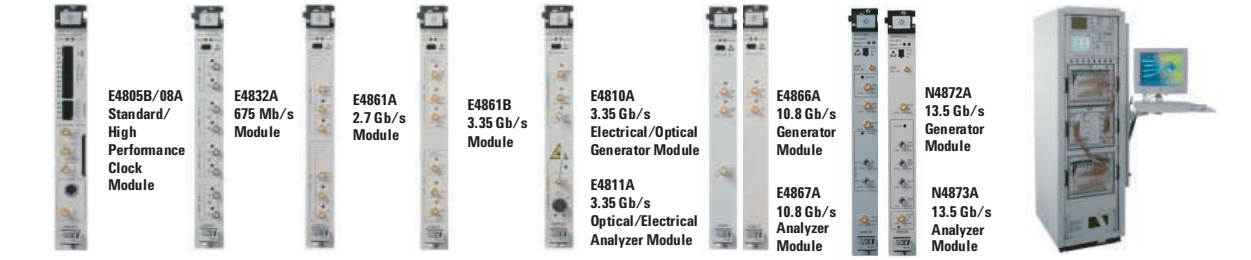
Agilent ParBERT 81250 is particularly suitable for the following applications:

1. 10GbE device testing
2. Multiplexer and Demultiplexer Test
- OC-768 device testing: You can test 16:1 and 4:1 40G devices using the ParBERT 81250 45G and either 3.3 Gbit/s or 10.8 Gbit/s modules
- OC-192 device testing: The ParBERT 81250 10.8 Gbit/s modules enable testing of the serial high-speed side of Muxes/DeMuxes. Combined with 675Mbit/s, 1.6Gbit/s, 2.7Gbit/s or 3.3 Gbit/s modules you can test both sides of multiplexers/demultiplexers
- OC-48 device testing

3. Characterization of SAN ICs
4. Manufacturing Test of multiple Transmitters, Receivers, Transceivers and Amplifiers
5. FEC Device Test

For more information on these applications, please see brochure p/n 5968-9250E. For information on the Agilent ParBERT 81250 45 Gbit/s, please see p/n 5988-3020EN. For more information on ParBERT 3.35 Gbit/s optical/electrical mod-ules, please see p/n 5988-5901EN. This document focuses on the ParBERT platform up to 10.8 Gbit/s.

Modules



Front Ends

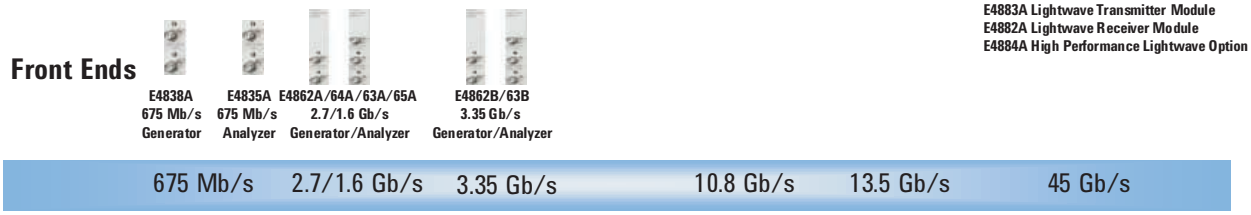


Figure 1: ParBERT Product Family

ParBERT 81250 Key Features & Benefits

Features	Benefits
Modular, flexible and scalable platform architecture · Up to 128 channels @ 675 Mbit/s · Up to 64 channels @ 3.35 Gbit/s, 2.7 Gbit/s · Up to 30 channels @13.5 Gbit/s, 10.8 Gbit/s	· Grows with customer's test and application needs · Covers a wide range of technologies and applications
Generator and Analyzer modules available from 675 Mbit/s up to 45 Gbit/s	Allows the configuration of a system to fit the customer's application needs
Mix of channels (generator/analyzer) and speed classes	Provides unique flexibility to test complex devices with many channels and/or frequencies, e.g. Serial bus applications, Mux/Demux (SerDes), FEC
Generate pseudo random word sequences (PRWS) and standard PRBS up to 2^{31}-1; Analyze bit error ratios with user-defined data, PRBS or mixed data from parallel ports	Perform parallel BER measurements - ideal for Mux/Demux applications
Generate and analyze single-ended, low voltage and differential signals - including true differential	· Test logic technologies e.g. LVDS, ECL, PECL, SSTL-2 · Generate the necessary signals to perform margin tests, emulate frequency and level changes and stress your device as far as possible
Data generation and analysis with sequencing and looping	· Generate complex sequences that contain memory-based (up to 32Mbit) and/or PRBS/PRWS data · Generate data packets with header and payload · React to control signals from the DUT
Auto phase & auto delay alignment	· Auto alignment of expected data with incoming data · Save time as you do not need to find the correct sample point manually - typically takes just 100ms, so ideal for manufacturing
Each generator or analyzer channel has independent programmable control of voltage levels and timing delay	Allows device characterization for a wide range of technologies/applications in the semiconductor and communication industry
Interrupt-free change of analyzer delay/generator delay (13.5 Gbit/s and 3.35 Gbit/s; other speed classes generator only)	Continuous running signals for measurements where changing analyzer delay is necessary
Jitter modulation (13.5 Gbit/s and 3.35 Gbit/s)	Allows jitter tolerance testing to be performed
Variable Cross (13.5 Gbit/s and 3.35 Gbit/s)	Provides real-world stress
Windows® 2000/NT 4.0 based user software	Provide "standard" and "detailed" views for performing measurements fast and efficiently
Plug and play drivers	Allows remote access and simplifies remote program development
Measurements Suite	· DUT output timing measurement - bathtub curve with jitter analysis (RJ/DJ separation), skew between channels, setup and hold times · Output level measurement - amplitude information, high/low level and Q-factor · Eye opening measurement - color and contour plots · Fast eye mask measurement - automatic threshold adjust, fast and efficient insights for manufacturing test · Comprehensive BER measurement - actual and accumulated BER, errors of ones and zeros, total bits transferred and file capturing for post-processing analysis.

Key Features (continued)

Perform Parallel BER measurements up to 13.5 Gbit/s

ParBERT 81250 makes testing of Mux/Demux (serializer/deserializer) devices easier. Only ParBERT 81250 is able to generate pseudo-random-word sequences (PRWS) on the parallel side and analyze bit-error-ratios with user-defined patterns, PRBS up to 2^{31}-1 or both combined.

PRBS/PRWS and memory capability

The polynomial 2^n-1, the PRBS algorithm and the parallel bus width define PRWS. The bits of the PRWS are assigned to parallel lines and are then multiplexed to form a PRBS (see figure 3).

Auto phase and auto delay alignment

As the latency from the input to the output is often not known exactly, or it is not deterministic, synchronization between incoming data and outcoming data has to be carried out. ParBERT 81250 has three capabilities to synchronize/align the incoming data automatically (see figures 4 and 5):

1) Data shift bit-by-bit if PRBS is used

2) Detect Word if user-defined patterns are used

3) Moving of the sampling point delay of the analyzer up to 10ns without stopping the instrument. Moving of the sampling point delay can also be used in addition to the alignment of data patterns (1 and 2) to refine the synchronization.

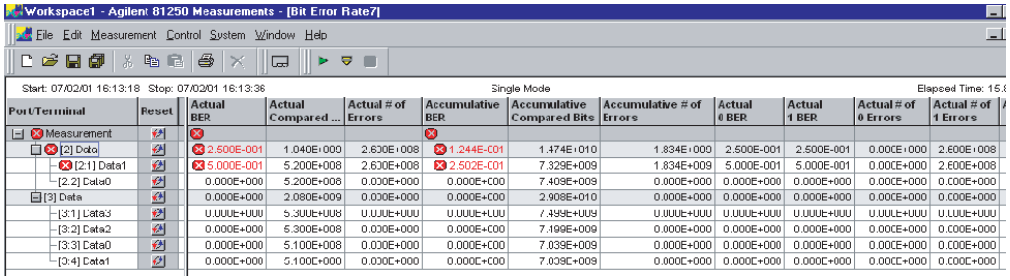


Figure 2: BER results screen

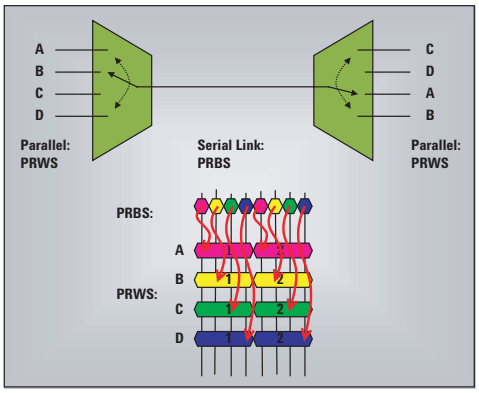


Figure 3: MUX/DEMUX Application: Relationship between PRBS and PRWS

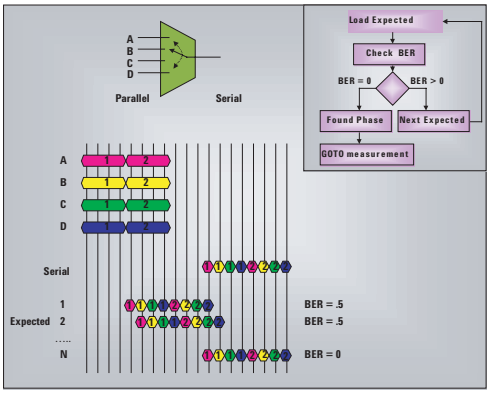


Figure 4: Mechanism of auto-phase and auto-delay assignment

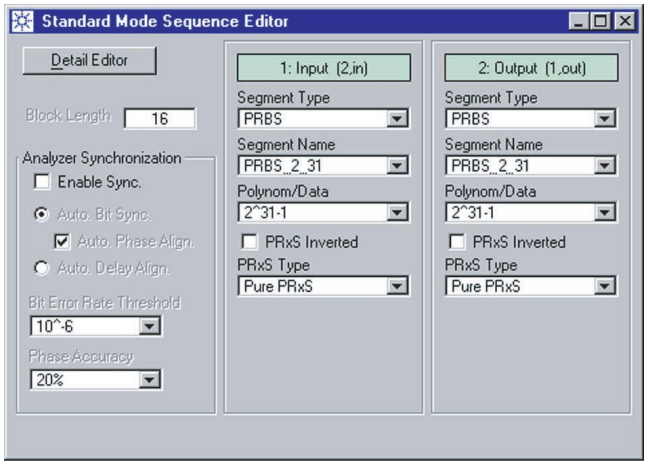


Figure 5: Standard view when choosing PRBS/PRWS patterns and data synchronization mode

Interrupt-free change of analyzer delay

The analyzer delay can be changed ±1 period whilst the instrument is running without causing it to stop see figure 6. The 13.5 Gbit/s and 3.35 Gbit/s modules can do this on the Analyzer and Generator.

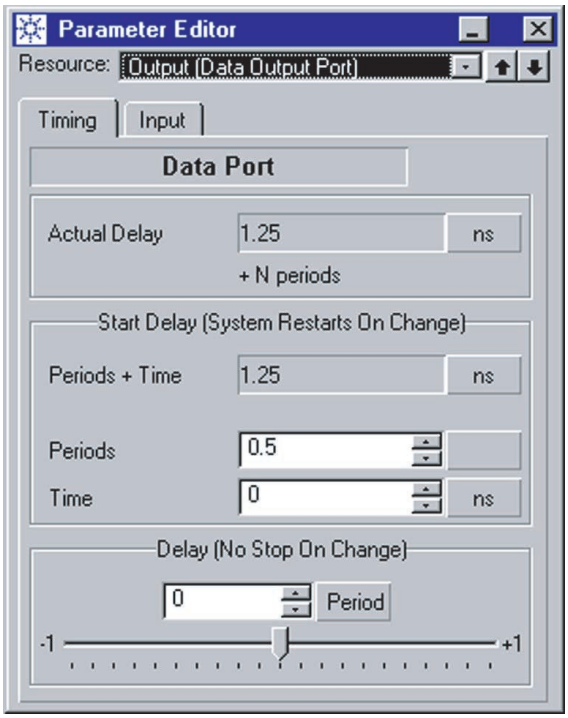


Figure 6: Parameter Editor for analyzer timing

Multiple frequencies

The modular architecture of ParBERT allows the use of different channels at different speeds. Therefore it is possible to combine channels of different speed classes in one ParBERT system. A ParBERT system can be configured with one or more clock groups. Each clock group is controlled from one clock module. Within one clock group (one clock module controls a group of channels) a frequency ratio of 2^n, n =1,2,....10 is possible, see figure 7.

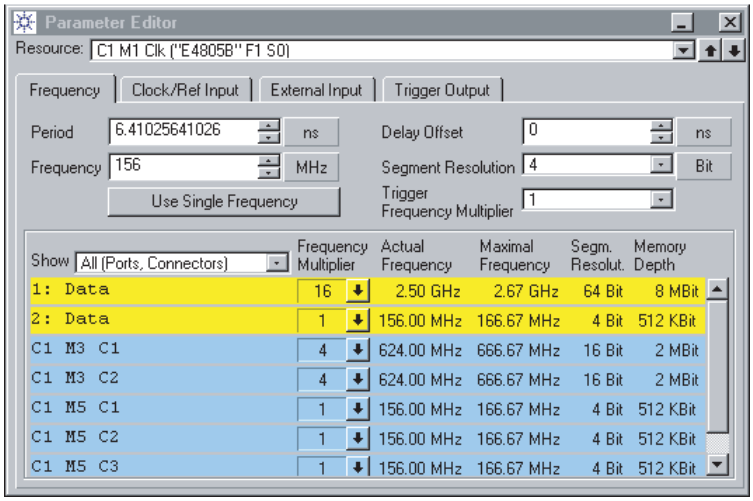


Figure 7: Parameter Editor for setting multiple frequencies in one system

With the two clock groups any frequency ratio m/n, n=1,2,...,256 is possible. The 'application examples' show some 'two-clock-system' configurations

Fundamental Platform Description

The idea of the ParBERT 81250 product structure is that you receive the instrument, which meets your measurement needs exactly. The ParBERT modularity offers modules and frontends. At 13.5 Gbit/s and 10.8 Gbit/s there are dedicated modules for Generators and Analyzers. At 3.35 Gbit/s, 2.7 Gbit/s, 1.6 Gbit/s and 675 Mbit/s the modules carry 2/4 front-ends. The **front-ends** determine which kind of output or input connectors your specific instrument has. This means front-ends determine the speed and input/output capabilities of your instrument. A mix of front-ends is possible within the modules. The front-ends are placed in **data modules,** which are responsible for sequencing, generating and analysing of data patterns including PRBS/PRWS. These modules, plus at least one **clock module,** which generates the common system frequency of the instrument, are installed in the mainframe.

The VXI frame offers 13 slots. Assuming the use of the FireWire interface and one Clock module in place, the mainframe can hold up to 10 channels at 13.5 Gbit/s, 11 channels at the data rate of 10.8 Gbit/s, 22 channels at 3.35 Gbit/s, 2.7 Gbit/s and 1.65 Gbit/s or 44 channels at 675 Mbit/s. If more channels are needed there is the possibility of adding up to two expander frames to reach the maximum number of channels within one clock group. Additional clock modules are needed to set up systems which work with different clock speeds that are not divisible or multipliable by the factors 2, 4, 8, 16 (if E4832A is used) and 2 and 4 (if E4861A is used). For example, for testing 1:7 or 1:10 Mux/Demux devices two clock modules are required. Please check the Application Examples within the next chapter.

The ParBERT **81250 Software Suite** runs on an external PC, or a laptop, which is connected to the system via an IEEE 1394 PC link to VXI. The operating system is MS Windows® NT 4.0 or Win 2000. The ParBERT 81250 Software Suite consists of:
- Graphical User Interface
- Measurement Suite
- Software Tools (10GbE Tool, SONET/SDH Frame Generator
- VXI Plug & Play Driver

At runtime the software consists of several processes, see new figure. The firmware server controls the hardware and is the link between the graphical user interface and the Hardware Modules. Also the Measurement Software or any custom remote program can communicate with the Firmware Server. The remote access is established either by using the Plug and Play drivers from Agilent Vee or from a C/C++/Visual Basic program or by a SCPI based language via GPIB. This allows the building of a customized VXI system including other standard VXI modules.

Table 6 gives an overview on key specifications of the different speed classes:

	675 Mbit/s	2.7 Gbit/s/3.35 Gbit/s	10.8 Gbit/s	13.5 Gbit/s
Data Rate Range	333.3 Kbit/s .. 675 Mbit/s	333.4 Mbit/s .. 2.7 Gbit/s 20.8 Mbit/s .. 3.35 Gbit/s	9.5 .. 10.8 Gbit/s	500 Mbit/s .. 13.5 Gbit/s
Number of Channels within 1 Frame / + 2 Expander Frames with ext. PC	44/132	22/66	11/33	10/30
Inputs/Outputs	differential & single ended	differential & single ended	differential & single ended	differential & single ended
Data Capability	PRBS/PRWS/ 2 Meg Memory	PRBS/PRWS/ 8/16 Meg Memory	PRBS/PRWS/ 32 Meg Memory***	PRBS/PRWS/ 64 Mbit Memory
Generator Formats	DNRZ, RZ, R1	2.7G:DNRZ 50% clock DNRZ, R1, RZ	DNRZ, separate clock output**	NRZ, DNRZ
Technology addressed	TTL, (P)ECL, LVDS	CML, (P)ECL*, LVDS, SSTL-2	CML, ECL,LVDS, SSTL-2	LVDS, CML, PECL, ECL, low voltage CMOS

Notes: * for PECL a BIAS Tee at Analyzer input is needed
**** separate clock output is single ended only**
***** balanced pattern only**

Table 6: Key Specifications of ParBERT channels

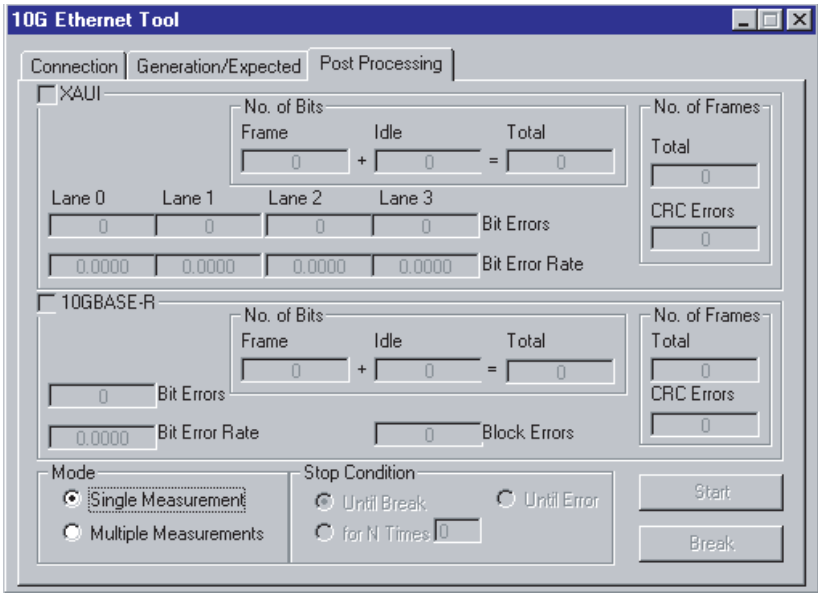


Figure 7b: 10GbE Processing Tool

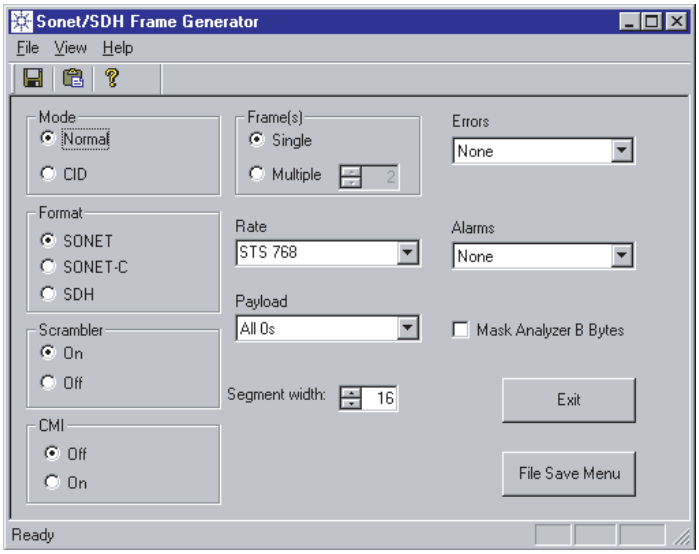


Figure 7c: SONET/SDH Editor

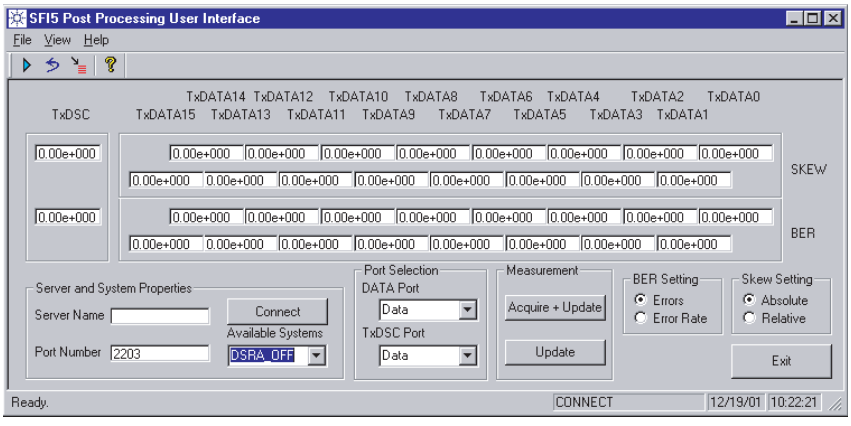


Fig 7d: SFI5 post processing

Analyzing the data & the DSC (17th) bit:

- Ensure that the 16 data channels are valid (valid PRBS 2^7-1 or 2^{11}-1) streams:
- Ensure that the 16 data channels are within skew specification.
- Ensure that the DSC (17th) bit is valid:
  - correct header
  - match to the 16 data channels

Measurement Software

The ParBERT measurement software includes the following measurements:
1. BER Measurement
2. Fast Eye Mask Measurement
3. DUT Output Timing Measurement
4. DUT Output Level Measurement
5. Eye opening

The ParBERT 81250 measurement software is a ready-to-use measurement user interface, which aids you with the verification and characterization of high-speed digital components and modules.

The measurement software offers three different levels of measurement analysis:
1. Fast pass/fail measurements ideal for production.

If you work in production you can test against limits, e.g. the BER is set at a given threshold. The fast pass/fail measurements allow you to test devices at up to ten times faster than with previous test methods - it typically takes less than one second!

2. Fast clock out to data out (setup and hold times), skew and eye opening specification results - no need to calculate values
3. Graphical results for detailed root cause analysis - see trends clearly and fast, e.g. pseudo color plot and contour plots.

If you are in R&D you can characterize your device under test (DUT), find the limits and specifications of the DUT and results can be viewed graphically.

With its easy-to-use Windows® 2000 or NT 4.0 based GUI and graphical results, it simplifies test development and allows easy test execution. Data can be exported and the graphical and numerical results printed.

Table 1: General	
	workspace
Store/recall	Single Measurements
Copy/paste	Measurement data to compare between measurements
Print	
Export of	Measurement data (ASCII)
On line help	
Remote interface	P&P Driver, Ready to use active X components to integrate complete measurements easily in VEE, Visual C++, VB, Labview, Mathlab and Excel

You can create test executive around the measurement software using Agilent Vee, National Instruments' LabVIEW®, Excel, Agilent TestExec, C/C++ and Microsoft® VisualBasic.

The Measurement Software is included in the standard software package which comes with each ParBERT 81250 system.

BER Measurement

The Bit Error Ratio measurement measures the total number of bits transferred and the number of errored bits, bits which don't meet the decision threshold. You can now view the actual 0 and 1 BER, actual 0 and 1 errors, accumulative 0 and 1 BER and accumulative 1 and 0 errors at once. The Bit Error Rate measurement can be run as a single shot or repeatedly.

Several run and error counting options and stop criteria can be defined. Repetitive mode offers automatic resynchronization. It is the ideal mode for characterizing your device, so good for R&D, for example, you can change the temperature and measure how it affects the BER. Single mode is particularly useful for manufacturing as you can stop the measurement after a specified number of errors and/or seconds.

Measurement results provided:
· Displayed errored ones and zeros at the same time
· Log file
· Resynchronization
· Pass/fail results

Table 2: BER Measurement	
Measurement Parameters	BER Compared bits Errors from expected 0s Errors from expected 1s Total errors Parameters from last measurement period Accumulated parameters
Measurement mode	Single or repetitive Repetition rate is programmable in seconds (In this mode resynchronization can be enabled)
Pass/fail	For actual and accumulated parameters
Log file	Logs all measured parameters

Fast Eye Mask

The fast eye mask measurement is ideal for use in manufacturing as a measurement typically takes just one second (including synchronization). This measurement records the BER of a pre-defined number of points (1 to 32), not the whole eye, defined by a threshold and timing value relative to the starting point of the measurement. You enter the pass/fail criteria of the measurement and the BER threshold, find the middle point of the eye with the sequence and then run the BER. For example, you can define a threshold and ParBERT will find the optimal sample point and the high and low levels automatically, e.g 20% and 80%.

Measurement results provided:
· BER at pre-defined sample points
· Pass/fail results

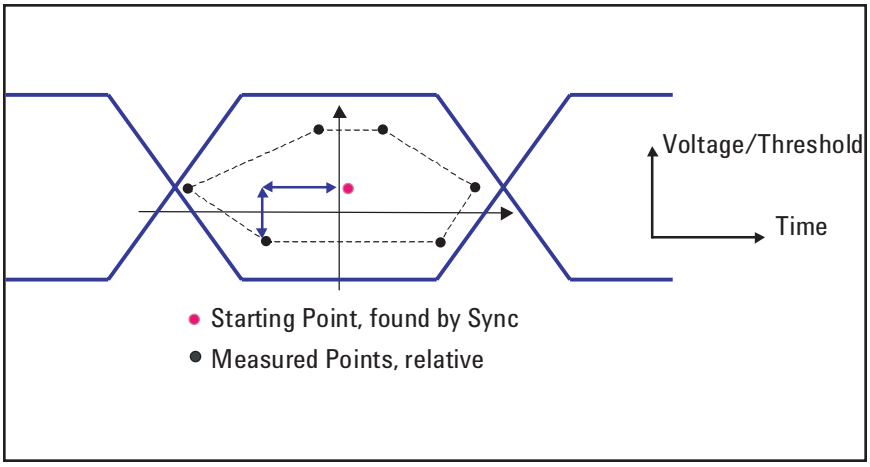


Figure 8: How the Fast Eye Mask measurement works

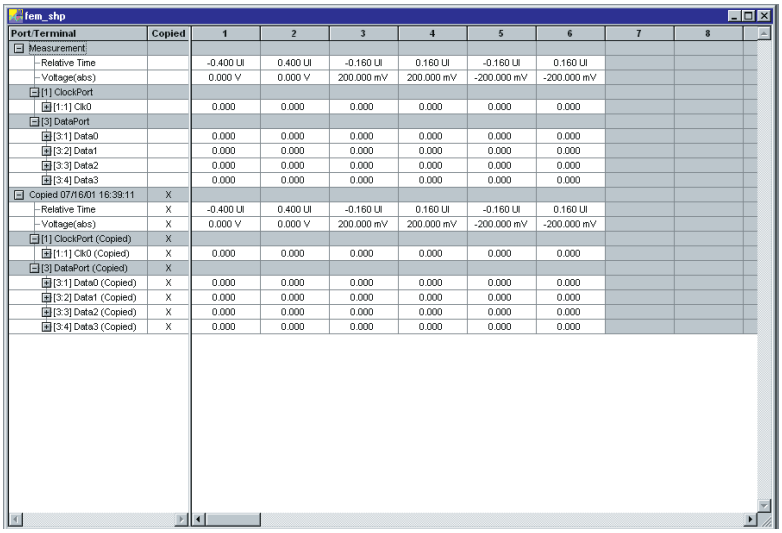


Figure 9: The Fast Eye Mask set-up and results window

Frequency	# channels	# points measured	Compared Bits	Time Taken
2.7Gbit/s	2	6	10^6	< 1 sec
2.7Gbit/s	2	32	10^6	~ 1 sec
675 MHz	16	6	10^6	~ 6 sec
675 MHz	16	32	10^6	~ 6 sec

Table 3: Fast Eye Mask measurement time examples (run on a system via IEEE 1394 PC link)

DUT Output Timing Measurement

This measurement measures the BER of a DUT's output versus sample point delay, which is shown graphically as a bath tub curve. The delay is always centered to the optimum sampling delay point of the port (terminals). If a clock is defined the clock to data alignment is measured. If the absolute delay can be measured it will also be displayed. Relative timing, where edges are compared, is also possible.

Measurement results provided:
- Clock out to data out timing relations (setup/hold time)
- Skew between outputs
- Delay at optimum sample point
- Phase margin
- Pass/fail results
- Jitter results for total jitter, random jitter and deterministic jitter

There is also a numerical view that shows the "numerical return values" for the selected BER threshold only.

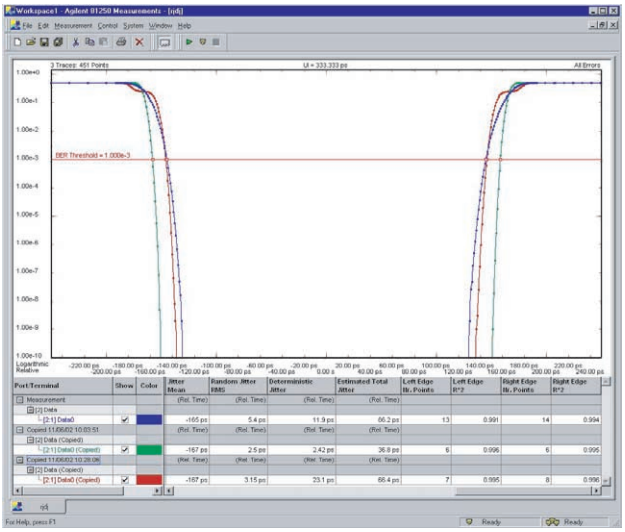


Figure 10a : View the DUT output measurement results as a bathtub curve

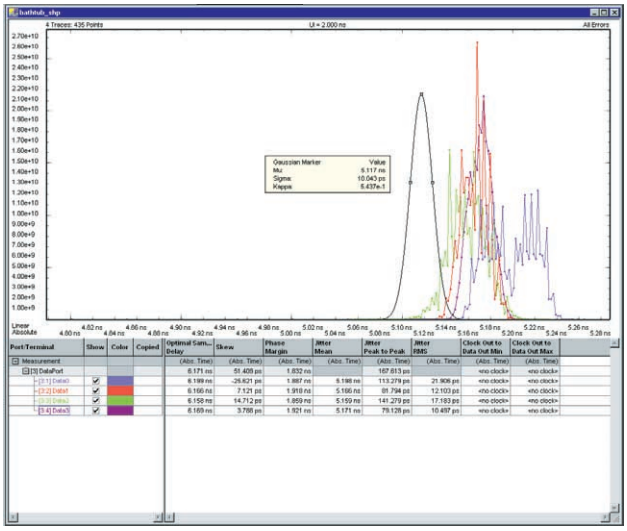


Figure 10b: Jitter can be directly equated from the bathtub curve. View the jitter as a histogram.

Table 4: DUT Output Timing Measurement	
Timing Parameters	Optimum sample point delay Phase margin Clock to data out min Clock to data out max Skew between channels
Jitter Parameters	RMS Jitter Mean Value Peak Peak Jitter for specific BER
Pass /fail	For all timing and jitter parameters Each parameter can be individually enabled
Graph	View of BER versus sample delay 2 Markers: delay, BER

Output Level Measurement

This measurement performs a sweep of the analyzer threshold. It is shown graphically as a bathtub curve, with the threshold on the Y-axis and BER on the X-axis (see figure 11a). From the data a histogram showing BER versus threshold can be derived (figure 11b) which can be used to calculate one/zero level means and standard deviations. Also a graph showing Q-factor from BER versus threshold (figure 11c) can be derived, which shows the result of two tail fitting operations for the innermost gaussian distributions in the BER histogram.

Table 5a Output Level Measurement	
Measurement Parameters	High/low level Mean level Amplitude Threshold margin High/low level standard deviation Peak peak noise Signal/noise ratio (rms & peak-to-peak) Q factor
Pass/fail	For all parameters Each parameter can be individually enabled
Graphs	BER versus threshold BER histogram versus threshold, Q from BER versus threshold

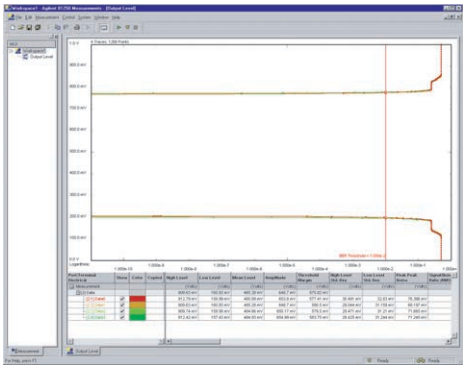
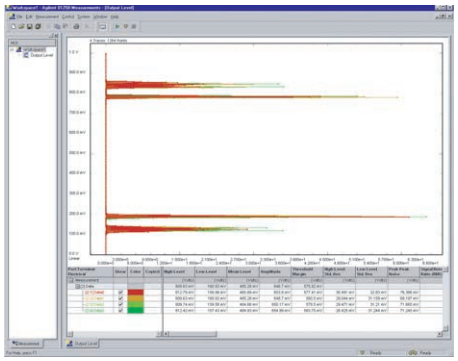
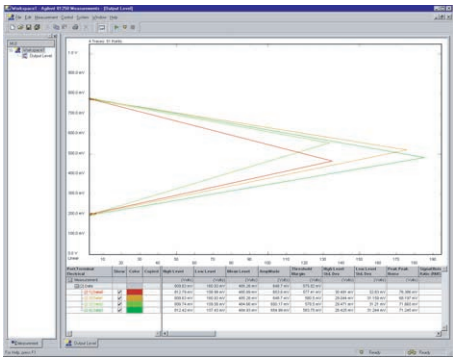


Figure 11a) BER versus threshold



11b) BER Histogram versus threshold



11c) Q from BER versus threshold

Eye Opening

To measure the eye opening the sampling delay and the threshold of the receiving channels are swept.

Measurement results provided:
- Eye opening (voltage and timing)
- Optimum sample point

Table 5b: Eye opening	
Meas. Parameters	Optimum sample point delay Optimum threshold Eye opening (Volt) Phase margin
Pass/fail	For all parameters Each parameter can be Individually enabled
Graph	Two markers:Voltage, Delay, BER

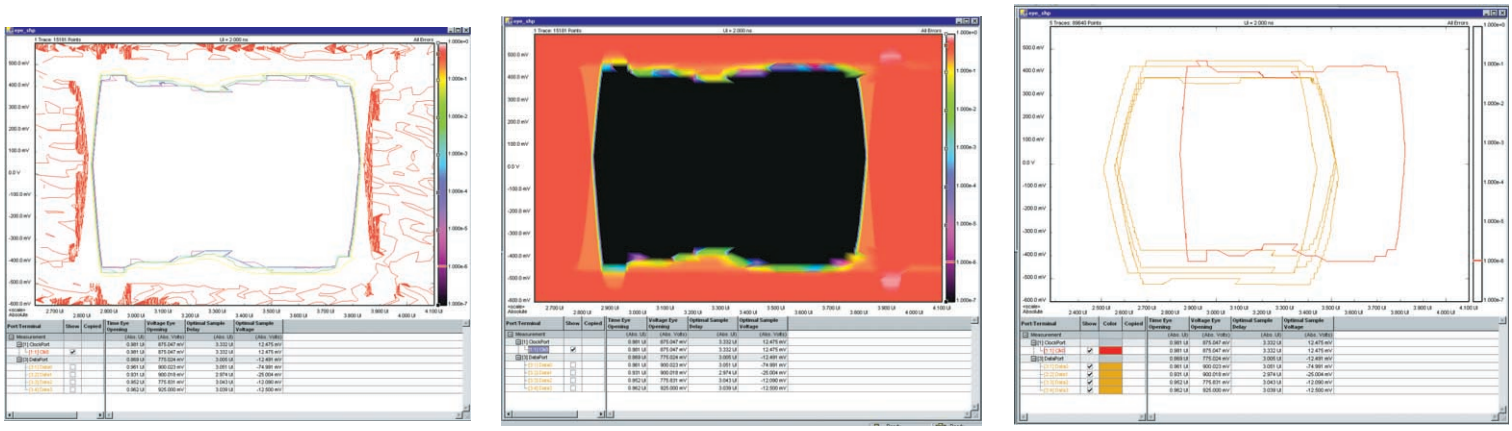
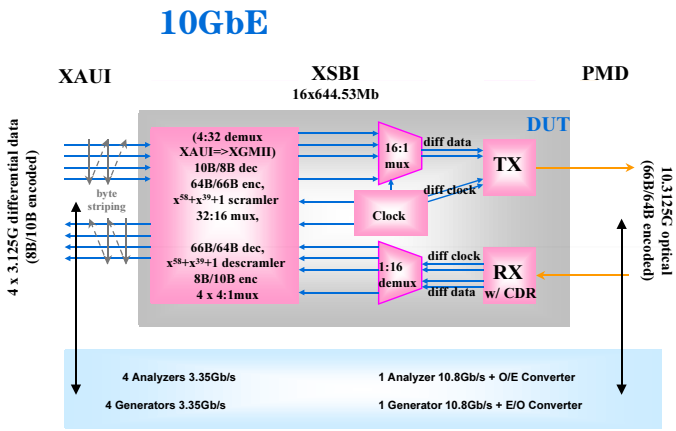


Figure 12 a/b/c: View the BER for one terminal as a pseudo color plot or contour plot or equal BER at BER Threshold

Application Examples



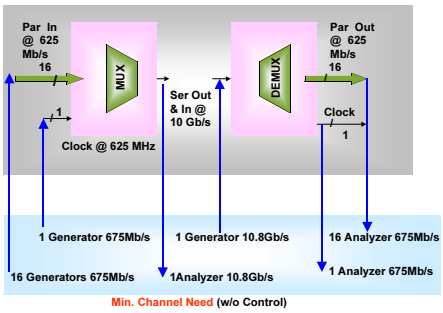
1x 81250A
1x 81250A-149
1x E4875A
1x 81250A-013
4x E4808A
4x E4861B
4x E4862B
4x E4863B
1x E4866A
1x E4867A

Figure 14a: 10GbE

10GbE

10GbE parts are used in the MAN area. The DUT is a module with 4x 3.125Gb/s electrical inputs and outputs each and 1x 10.3125Gbit/s optical input and output. The DUT supplies a clock of 156.25MHZ to all Systems. The optical signals are converted electrically.

The configuration of ParBERT 81250 for 10GbE testing includes four clock groups and E/O and O/E converters for the optical signals at 10.3125Gbit/s.



1x 81250A
1x 81250A-149
1x 81250A-152
1x E4875A
1x 81250A#013
2x E4808A
10x E4832A
17x E4838A
9x E4835A
1x E4866A
1x E4867A
1x 11667B

Figure 15: OC 192 example

OC 192

OC 192 parts are used in telecom applications. Here the DUT consists of two chips, one TX and one RX. There is no clock at the serial side. For testing 16x 675 Mbit/s Generators and Analyzers on the parallel side are needed. The serial side needs 1 times 13.5 Gbit/s or 10.8 Gbit/s Generator and Analyzer.

The 81250 configuration to the left contains all necessary resources to test Mux/Demux. Both parts of DUT can be tested at one run-time, regardless of whether memory-based data or PRBS/PRWS are used.

The 13.5 Gbit/s or 10.8 Gbit/s channels can be used together with the 675 Mbit/s channels, as the multiplier is 16 (another multiplier would require separation into 2 clock groups, similar to the other two examples). The combination of all generators and analyzers in individual clock groups eliminates the synchronization limitations.

OC 768, 1:4 MUX / DEMUX

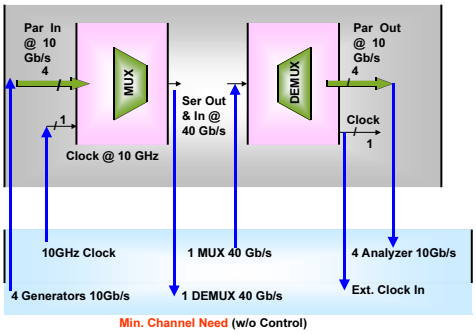


Figure 16: OC 768 example

1x E4896A
1x E4896A-002
1x E4897A
1x E8244A

OC 768, 1;4 Mux/DeMux ratio

DUT consists of two chips, one TX one RX. There is no clock at the serial side. This will require 4x 10.8 Gbit/s Generator and Analyzer channels for the parallel side and 1x 43.2 Gbit/s Generator and Error Detector Bundle E4894A and E4895A.

The 81250 configuration, shown in Figure 16, contains all necessary resources to test Mux/Demux. Both parts of the DUT could be tested at one run-time using PRBS/PRWS data

OC 768, SFI5 (1:17) MUX and DEMUX

with ParBERT 3.35G modules @ parallel

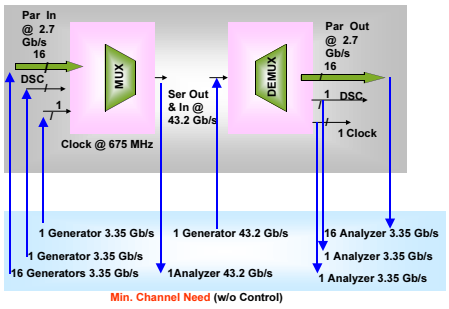


Figure 16a: OC 768 SFI-5 Mux and DeMux

1x 81250A
1x 81250A-149
1x E4875A
1x 81250A-013
2x 81250A-152
2x E4808A
18x E4861B
18x E4862B
18x E4863B
1x E4868A
1x E4869A
1x E8244A

OC 768, SFI-5 (1:17) Mux/DeMux

The DUT consists of two parts: a TX and RX part. Characteristic for SFI-5 is the 17th bit, called DSC signal. This carries specific timing alignment data. The modular ParBERT 81250 architecture allows the easy addition of a 17th generator and analyzer channel to handle the DSC signal.

The 81250 configuration, shown in Figure 16a, contains all necessary resources to test SFI-5 Mux and Demux. Both parts of DUT can be tested but not at one run-time. The parallel side (3.35 Gbit/s) includes 18 generators and 18 analyzers, so beside the 16 data bits, the test system can handle the DSC signal (17th bit) and any clock if necessary.

Gigabit Ethernet, 1:10 MUX / DEMUX

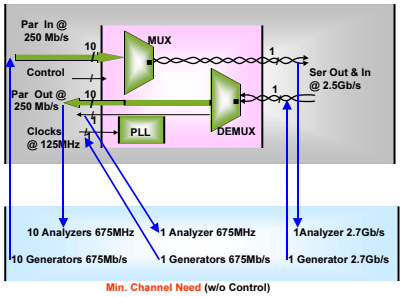


Figure 14: Gigabit Ethernet example

1x 81250A
1x 81250A-149
1x E4875A
1x 81250A-013
2x E4805B
6x E4832A
11x E4838A
6x E4835A
1x E4861A
1x E4862A
1x E4863A

Gigabit Ethernet

Gigabit ethernet tranceivers take care for physical transreceiving data between a PC and a local network. The implementation consists of one chip, containing one TX and one RX. There is no clock at the serial side.
(For 10 Gigabit Ethernet there would be signals running at 3.125 Gbit/s) For testing this device without the control inputs, 11x 675 Mbit/s Generator and Analyzer channels (1x Clock and 10x data) would be needed for the parallel side. On the serial side 1x 2.7 Gbit/s Generator and Analyzer are needed.

The 81250 configuration, shown in figure 14, contains all necessary resources to test Mux/Demux. As long as PRBS/PRWS data are used, both parts of the DUT can be tested at one run-time. If memory-based data is used, (due to synchronization limitations) only one part can be tested at one run time.

Video (DVI), 1:7 MUX / DEMUX

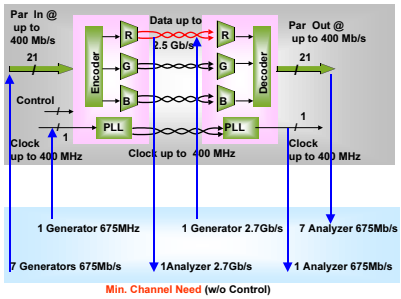


Figure 13: Video (DVI) example

1x 81250A
1x 81250A-149
1x E4875A
1x 81250A-013
2x E4805B
4x E4832A
8x E4838A
4x E4835A
1x E4861A
1x E4862A
1x E4863A

Digital video

For transferring data between CPU and Display, a digital video interface was created. The picture shown here is a simple example as there are several implementations created with more or less serial interconnections (up to 8). It is very common that the Mux/Demux ratio is 1:7 with all of these video interfaces. The DUT consists of two chips, one TX and one RX. Besides 3x serial there is also the clock at the speed of parallel side transferred.

For a minimum test of this device, the number of channels needed is counted to stimulate and analyze one of the three Mux/Demux paths. So this would need a total of 8x675 Mbit/s Generators and Analyzers (1x for clock, 7x for data) and 1x 2.7 Gbit/s Generator and Analyzer for the serial side.

The 81250 configuration, shown in figure 13, contains all necessary resource to test Mux/Demux. Testing is limited to one serial interface (either R, G or B). As long as PRBS/PRWS data are used both parts of DUT could be tested at one run-time. If memory-based data is used, (due to synchronization limitations) only one part can be tested at one run-time.

Signal Waveforms

The following waveforms are taken from the different speed classes of the ParBERT family.

The pictures are taken showing once the Generator output on the scope and second the Analyzer Inputs are connected to an ideal source and with the help of the eye opening measurement (page 9) the performance of the Analyzer is recorded.

ParBERT Settings:

Generator and Analyzer in single-ended mode, normal in/out used.

Frequency:
625 Mbit/s used for:
E4808A + E4832A + E4838A + E4835A

2.5 Gbit/s used for:
E4808A + E4861A + E4862A + E4863A

10.0 Gbit/s used for:
E4808A + E4866A + E4867A

Data:
PRBS 2^{23} -1 (stimulus and expected) data

Generator levels:
Low Level -.4V, High levels + .4V

Analyzer/Eye Opening:
Single-ended, terminated to ground

Compared Bits 10^6
BER Threshold 10^{-3}

Trigger Out: clock mode (625 MHz), levels O/1V

Scope settings:

Agilent 81600 DCA with 83484A 50 GHz module

· connected with 1m SMA cables
· external trigger from 81250 trigger out
· signal adjusted with Auto scale
· every measurement for 300 events

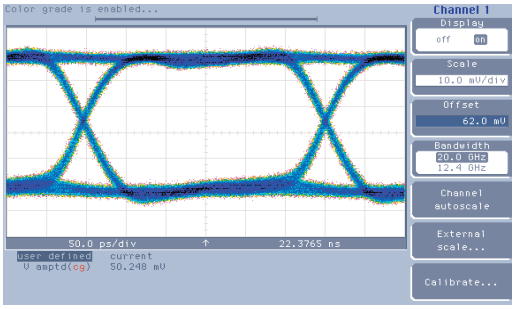
Ideal source:

for 675 Mbit/s, 2.7 Gbit/s, 3.35 Gbit/s:
transistion time 30ps,
jitter <10ps pp, levels -.5V/OV

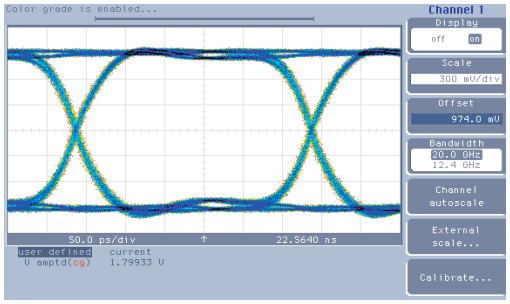
For 10.8 Gbit/s:
transition time 10ps
jitter <8ps pp, levels + - .4V

Eye plots

50mVpp @ 3.3Gbit/s



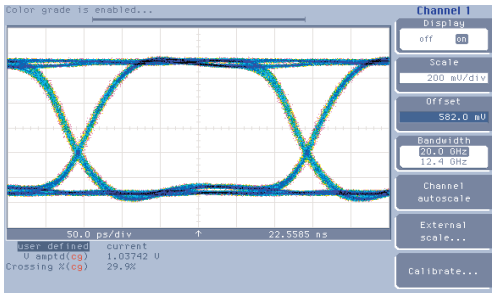
1.8Vpp @ 3.3Gbit/s



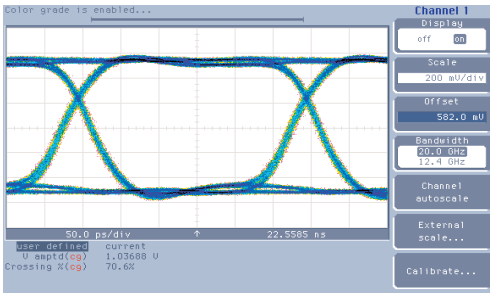
The 3.35 Gbit/s Generator Output is designed for clean and fast output signals. It offers a swing of 50mV to 1.8V within voltage window suited for testing LVDS, CML, (P)ECL and SSTL –2 technologies.

Crossing point

30% @ 3.3Gbit/s

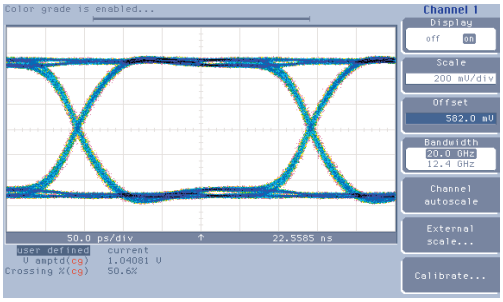


70% @ 3.3Gbit/s



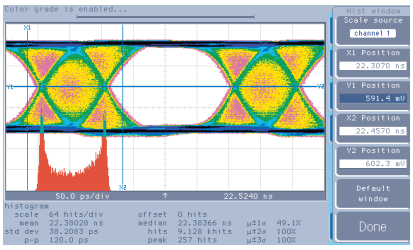
The 3.35 Gbit/s Generator allows a variable cross-over for differential signals. The cross-over can be programmed by the user interface or remote program between 30 to 70% .

50% @ 3.3Gbit/s

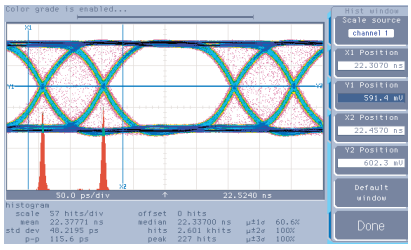


Jitter modulation@3.3Gbit

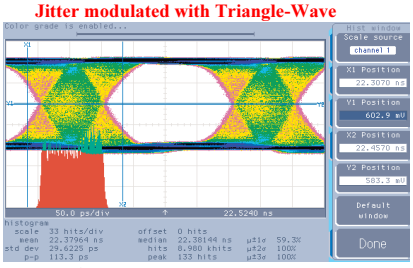
Jitter modulated with Sine-Wave



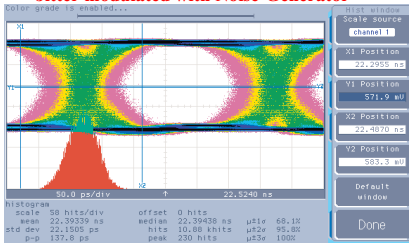
Jitter modulated with Rectangle-Wave



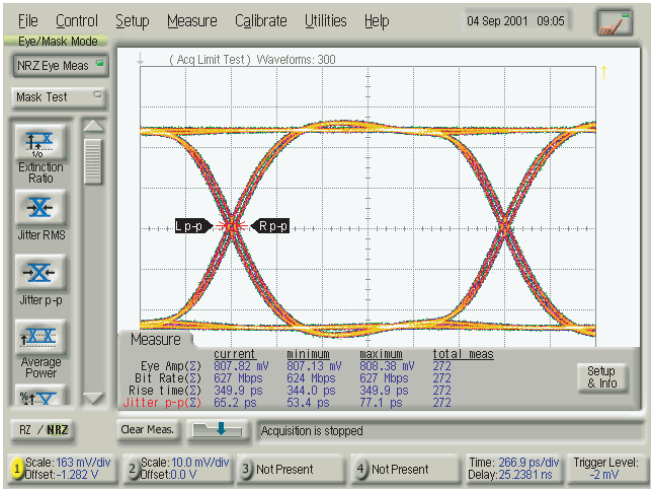
Jitter modulated with Triangle-Wave



Jitter modulated with Noise-Generator



The 3.35 Gbit/s Generator has a Control Input for modulating the Delay with the help of an external signal. This modulation can be used to emulate jitter. The picture shows this modulatioin for different types of control voltages. The modulation can be used to test a DUT for jitter tolerance.



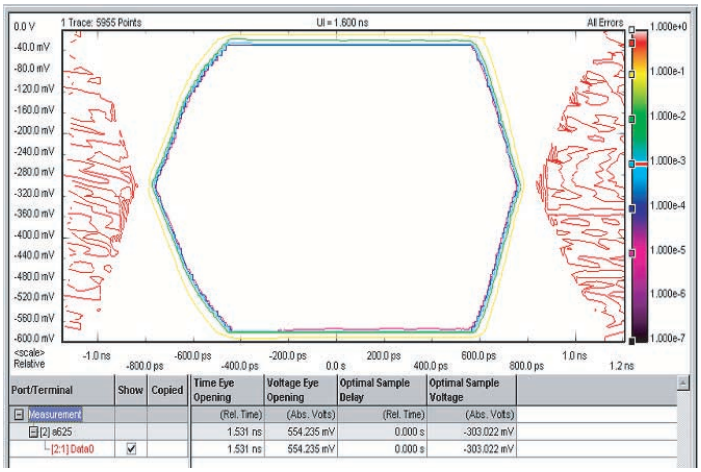
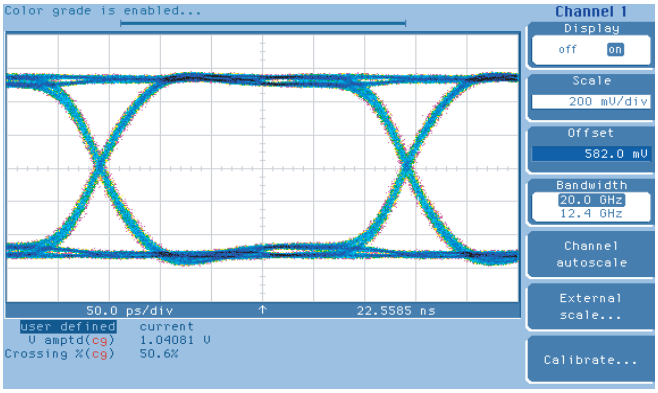


Figure 17a, b: Signals of E4832A with E4838A Generator and E4835A Analyzer



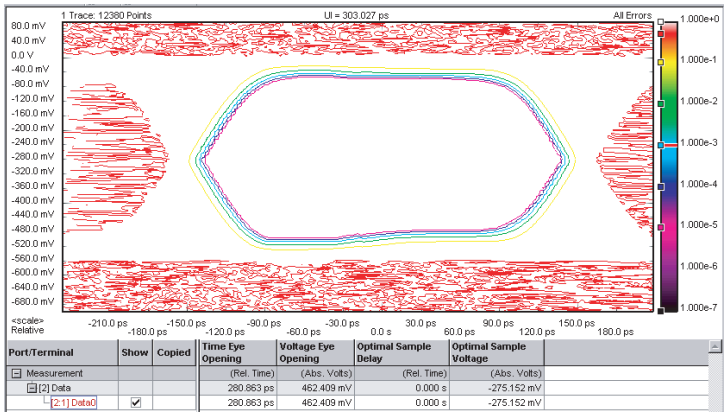
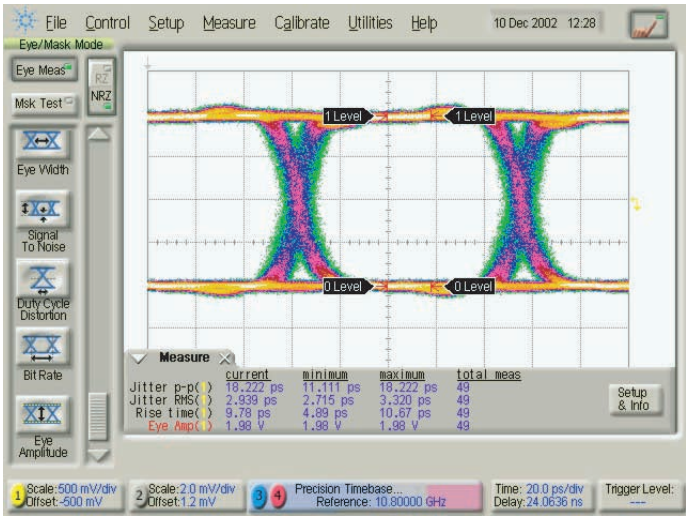


Figure 18a, b: Signal of E4861B with E4862B and E4863B Analyzer



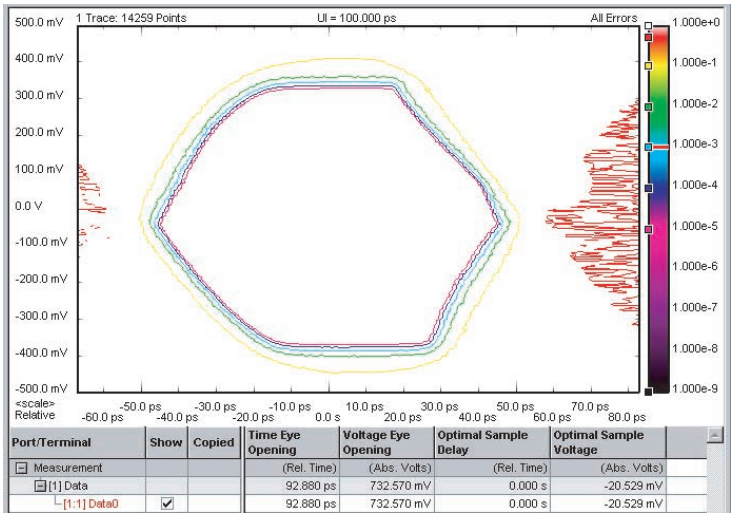


Figure 19a, b: Signal of E4866A Generator together with N4868A and E4867A Analyzer

Agilent N4872A ParBERT 13.5 Gb/s Generator
Agilent N4873A ParBERT 13.5 Gb/s Analyzer
Technical Specifications

Preliminary

Technical Specifications
All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10° to 40°C ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminate with 50 Ohms to ground at ECL levels if not specified otherwise.

General

The N4872A Generator and N4873A Analyzer modules are each one VXI slot wide and operate in a range from 500 Mb/s up to 13.5 Gb/s. Some restrictions may apply at data rates between 500 Mb/s and 666 Mb/s. The ParBERT 13.5 Gb/s modules require the E4809A 13.5 GHz Central Clock module. All specifications, if not otherwise stated, are valid at the end of the recommended N4910A cable set (24" matched pair (2.4mm).

The N4872A Generator module generates hardware-based PRBS up to 2^{31}-1, PRWS and user-defined patterns and provides a memory depth of 64 Mbit. The N4873A can synchronize on a 48bit detect word, or on a pure PRBS pattern without detect word.

Timing Specifications

The ParBERT 13.5 Gb/s modules are able to work with three different clock modes. The common clock mode is provided by the E4809A 13.5 GHz Central Clock module, which generates clock frequencies up to 13.5 GHz. The system also works synchronously with an external clock, which is connected to the E4809A clock module. Using the N4873A Analyzer module, CDR capabilities require the connecting of the Analyzer's CDR OUT to the E4809A clock module.

N4872A & N4873A

Table 1: N4872A Data Generator Timing Specifications (@ 50 % of amplitude, 50 Ohm to GND)	
Frequency range	500 MHz to 13.500 GHz
Delay = Start delay+Fine delay	Can be specified as leading edge delay in fraction of bits in each channel
Start Delay Range	0 to 100ns
Fine Delay Range	
Data Rate: >666Mb/s	±1Period (can be changed without stopping)
Data Rate: <=666Mb/s	1,5ns (can be changed without stopping)
Delay Resolution	100 fs
Accuracy	±10 ps ± 50 ppm relative to the zero-delay placement.
Relative Delay Accuracy	1ps + 2%
Skew between modules of same type	20 ps after deskewing at customer levels and unchanged system frequency.

Table 2: N4873A Analyzer Timing All timing parameters are measured at ECL levels, terminated with 50 Ohm to GND	
Sampling rate	Same as generator
Sample Delay	Sample Delay = start delay + fine delay
Start Delay Range	Same as generator
Fine Delay Range	Same as generator
Resolution	Same as generator
Accuracy	Same as generator
Skew	Same as generator

Sequencing

The sequencer receives instructions from the central sequencer and generates a sequence according to that. The sequencer can also run without the central sequencer, generating its own sequence. Therefore it is possible to have ParBERT 13.5 Gb/s channels generating different sequences. The channel sequencer can generate a sequence with up to 120 segments. The sequencer has 2 loop levels, which allow nested loops.

An analyzer channel generates feedback signals that can control the channel sequencer and/or the central sequencer. In the case of parallel analyzer channels, the feedback has to be routed to the central sequencer to allow a common reaction of all parallel channels. In the case of a single receive channel, the channel sequencer itself can handle the feedback signals.

Pattern Generation

The data stream is composed of segments. A segment can be made up of the memory-based pattern type, memory-based PRBS or hardware generated PRBS. A total of 64Mbit (at segment length resolution 512bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to 2^{15}-1 or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio. A zero substitution pattern extends the longest zero series by a user selectable number of additional zeroes. The next bit following these zero series will be forced to 1. Mark ratio is the ratio of 1s and 0s in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4 and 7/8.

Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 512 the number of repetitions is also 512. That means that a 2^{15}-1 PRBS uses up to 16Mbit of the memory. Hardware-based PRBS can be a polynomial up to a degree of 2^{31}-1. No memory is used, so the total memory is free for memory-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. In case of an error a bit will be inverted, so instead of a 0 a 1 is put out and vice versa.

Table 3: N4872A & N4873A Pattern and Sequencing	
Patterns:	
Memory based	
PRBS/PRWS	Up to 64Mbit
Marker Density	2^n-1, n= 7, 9, 10, 11, 15
Errored PRBS/PRWS	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n-1, n= 7, 9, 10, 11, 15
Extended ones or zeros	2^n-1, n= 7, 9, 10, 11, 15
Hardware based	
PRBS	2^n-1, n= 7, 10, 11, 15, 23, 31
PRWS Port width	1, 2 , 4, 8, 16
Analyzer Auto-synchronization	On PRBS or Memory-based Data Manual or automatic by: Bit synchronization with or without automatic phase alignment Automatic delay alignment around a start sample delay (Range: ±50ns) BER Threshold: 10^{-4} to 10^{-9}

N4872A Generator Module

The N4872A generates differential or single-ended data and clock signals operating from 500 Mb/s up to 13.5 Gb/s. The output levels are able to drive high-speed devices with interfaces like LVDS, ECL, PECL, CML and low voltage CMOS. The nominal output impedance is 50 Ohm typical. The Delay Control IN has a single-ended input with 50 Ohm impedance. The input voltage allows one to modulate a delay element up to 1 GHz DC (200ps) within the Generator's differential output.

Data OUT

Table 4: Parameters for N4872A ParBERT 13.5 Gb/s Generator		
Data Output	1, differential or single ended, 2.4mm(f)	**(1)**
Impedance	50 Ohm typ.	
Output amplitude/Resolution	0.05Vpp...2Vpp / 5mV	
Output voltage window	-2.00 to +3.00 V	
Accuracy HiLevel/Amplitude	±2%±10mV	
Short circuit current	80 mA max.	
External termination voltage	-2V to +3V	**(2)**
Data formats	Data: NRZ, DNRZ	
Addressable technologies	LVDS, CML PECL; ECL (terminated to 1.3V/0 V/-2 V) low voltage CMOS	
Transition times (10%-90%)	<25ps	
Jitter	< 7 ps peak-peak @BER 10E-3	
Cross-point adjustment (Duty cycle distortion)	20%...80% typ.	

(1) In single-ended mode, the unused output must be terminated with 50 Ohm to GND.
(2) External termination voltage must be less than 3V below V_{OH}. External termination voltage must be less than 3V above V_{OL}. Termination into AC is possible.

Clock OUT

Table 5: Parameters for N4872A ParBERT 13.5 Gb/s Generator		
Clock Output	1, differential or single-ended, 2.4mm(f)	**(1)**
Frequency	Same as Data Rate at Data OUT	
Impedance	50 Ohm typ.	
Output amplitude/Resolution	0.05Vpp...2Vpp/5mV	
Output voltage window	-2.00 to +3.00 V	
Accuracy HiLevel/Amplitude	±2% ±10mV	
Short circuit current	80 mA max.	
External termination voltage	-2V to +3V	**(2)**
Addressable technologies	LVDS, CML PECL; ECL (terminated to 1.3V/0 V/-2 V) low voltage CMOS	
Transition times (10%-90%)	<25ps	
Jitter	< 1 ps RMS @BER 10E-3	
SSB phase noise (10GHz@ 10kHz offset, 1Hz bandwidth)	target< - 75dBc with clock module E4809A	

(1) In single-ended mode, the unused output must be terminated with 50 Ohm to GND.
(2) External termination voltage must be less than 3V below V_{OH}. External termination voltage must be less than 3V above V_{OL}. Termination into AC is possible.

Delay Control IN:

Table 6: Parameters for N4872A ParBERT 13.5 Gb/s Generator	
Delay Control Input	Single-ended; DC-coupled; SMA(f)
Input voltage window	-250mV ... +250mV (DC-coupled)
Input Impedance	50 Ohm typ.
Data Rate (500MHz...13.5GHz)	
Delay Range	-100ps ... +100ps
Modulation Bandwidth	DC ... 1 GHz @ 10.3125 Gb/s

Data IN

Table 7: Parameters for N4873A ParBERT 13.5 Gb/s Analyzer		
Number of channels	1, differential or single ended, 2.4mm (f)	
Maximum Data Rate	13.5 Gb/s	
Input amplitude	50mVpp ... 2Vpp	
Input sensitivity		
Single-ended	Tbd mVpp typ. at 10Gb/s and PRBS 2^{31}-1 and BER < 10^{-12}	
Differential	Tbd mVpp typ. at 10Gb/s and PRBS 2^{31}-1 and BER < 10^{-12}	
Input voltage range	-2V ... +3V (selectable 2V window)	
Internal termination voltage (can be switched off)	-2.0 to +3.0 V (must be <3V below Input High Level)	
Threshold voltage range	-2.0 to + 3.0 V	
Threshold resolution	0,1 mV	
Threshold accuracy	±20 mV ± 1%	
Relative Threshold accuracy	Tbd	
Noise Level	Tbd mV	**(1)**
Minimum detectable pulse width	25ps typ.	
Bandwidth/Risetime	Tbd GHz/tbd ps.	
Phase margin (Source: N4872A)	> 1UI - 12ps (Data Rate >6.8GSa/s) > 1UI - tbd (Data Rate < 6.8GSa/s)	
Jitter	<tbd ps rms	
Impedance	50 Ohm typ. (100 Ohm differential, if termination voltage is switched off)	

(1) Input terminated with 50 Ohm to GND.

N4873A Analyzer Module

The analyzer features are:
- Acquire data from start
- Compare and acquire data around error
- Compare and count erroneous ones and zeros to calculate the Bit-Error-Rate.

Receive memory for acquired data is up to 64Mbit deep, depending on segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum Mux-factor (16, 32, 64, 128, 256, 512).

The analyzer is able to synchronize on a received data stream by means of a user selectable synchronization word. The sync word has a length of 48 bits and is composed of 0s, 1s and Xs (don't cares). The detect word must be unique within the data stream. Synchronization on a pure PRBS data-stream is done without a detect-word, instead by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ohm impedance. The sensitivity of 50mV and the common mode range of the comparator allow testing all common differential high-speed devices. The user has the choice of using the differential input with or without termination voltage or as single ended input (with termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

Clock Data Recovery

The Analyzer module has integrated CDR capabilities, which allow the recovery of either clock or data. Before the CDR can lock on the incoming data stream, the data rate must be defined within the user interface; common data rates are pre-defined. In CDR mode, phase alignment to the center of the eye is done automatically during synchronization. To ensure correct operation, the CDR Output must be connected to the Clock Input of the E4809A 13.5 GHz Central Clock module.

Frequency Restrictions

Data rates between 500 Mb/s and 666 Mb/s can be used with the following restrictions:

- No synchronous start
- No deskew possibility
- Synchronization is limited to bit sync.
- No automatic delay adjust
- No phase adjust.

Table 8: Parameters for N4873A ParBERT 13.5 Gb/s Analyzer - Clock Data Recovery

Common Data Rates	OC-192:	9.953Gb/s
	10GbE:	10.3125Gb/s
	Fiber Channel:	10.51875 Gb/s
	G.709/G.975:	10.664Gb/s / 10.709Gb/s
	S-ATA/FireWire:	6.4Gb/s
	PCI-Express:	6.4Gb/s
	OC-48:	2.488Gb/s
	10GbE:	3.125Gb/s
	SAN:	3.187Gb/s
	S-ATA/FireWire:	3.2Gb/s
Frequency Ranges	9.9GHz ...10.9GHz	
	4.9GHz ... 6.42GHz	
	2.45GHz ... 3.21GHz	
Lock Time	<100.000 Bits (PRBS 2^{23}-1)	
Output Jitter (Clock at Aux Out)		
Data Rate: 9.9Gb/s ... 10.9Gb/s	0,02UIrms typ. measured @ 10.3125Gb/s	
Data Rate: 4.9Gb/s ... 6.42Gb/s	0,02UIrms typ. measures @ 6.4Gb/s	
Data Rate: 2.45Gb/s ... 3.21Gb/s	0,02UIrms typ. measured @ 3.125Gb/s	
Bandwidth		
Data Rate: 9.9Gb/s ... 10.9Gb/s	> 4.5MHz; slope 20dB/decade	
Data Rate: 4.9Gb/s ... 6.42Gb/s	> 3.6 MHz; slope 20dB/decade	
Data Rate: 2.45Gb/s ... 3.21Gb/s	> 1.875MHz; slope 20dB/decade	

E4866A ParBERT 10.8 Gb/s Generator Module
N4868A ParBERT Booster Module
E4867A ParBERT 10.8 Gb/s Analyzer Module
Technical Specifications

E4866A/E4867A

There is one module E4866A for Generator 10.8 Gbit/s and one module E4867A for Analyzer 10.8 Gbit/s. N4868A is a Booster Module for E4866A generator.

Clock Timing

The generator provides complementary data and single ended clock output. Both clock out and data out can be moved with the variable delay, but it is the same delay for both. The analyzer has also a variable sampling delay. This consits of two parts: once the start delay with a large range and second the time delay of the ±1 period without stopping.

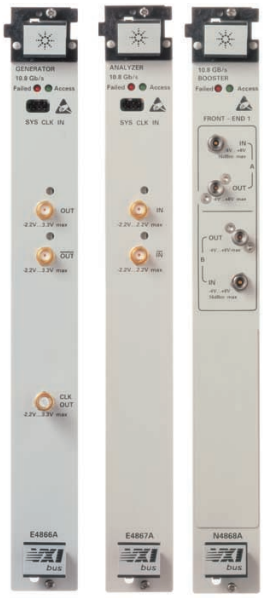
Data capabilities

PRBS/PRWS and memory-based data are defined by segments. Segments are assigned to a generator for a stimulating pattern. On an Analyzer it defines the expected pattern where the incoming data are compared to. The expected pattern can be setup with mask bits. The segment length resolution is the resolution to which the length of a pattern segment can be set. The segment length resolution is 256 bits for a total of 32 Meg memory.

AC coupling behind sampling circuit

The AC coupling does not impact the performance of the analyzer as long as the input data is balanced or the following limitations are not exceeded:

1. For infinite time period a mark density from 9/10 to 10/9 is tolerated.
2. All zero or all one patterns must not be longer than 20000 bits or 2 us.
3. When data recovers from imbalanced pattern to a balanced pattern a settling time of max. 200us takes effect.



E4866A/ E4867A/N4868A Modules

Table 1: E4866A Timing Specifications (@ 50 % of amplitude, 50 Ohm to GND)	
Data range	9.5 Gbit/s to 10.8 Gbit/s
Clock range	9.5 GHz to 10.8 GHz
Delay Range	0 to 300 ns
Delay Resolution	1 ps
Accuracy	±20 ps ± 50 ppm relative to the zero-delay placement.
Skew between modules of same type	50 ps typ. after deskewing at customer levels and unchanged system frequency

Table 2: E4866A Pattern and Sequencing	
Segment length resolution	256bits
Patterns:	
Memory based	up to 33,554,432bits
PRBS/PRWS	2n-1, n= 7, 9, 10, 11, 15, 23, 31
Marker Density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n-1, n=7, 9, 10, 11, 15
Errored PRBS / PRWS	2^n-1, n= 7, 9, 10, 11, 15
Extended ones or zeros	2^n-1, n= 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4,

Table 3: Parameters for Clock output E4866A 10.8GHz	
Output	1, single ended, AC coupled, to be used into 50 Ohm
Duty cycle	50% typical;
Maximum external voltage	-2.2V to +3.3 V
Amplitude/Resolution	0.5Vpp fixed typ.
Transition times (20%-80%)	sine wave
Clock Jitter	< 2ps RMS

Table 4: Parameters for Data output E4866A 10.8 Gbit/s with N4868A Booster *		
Outputs	1, differential, 50 Ohm typ.	1, differential or 2, single ended
Data formats	NRZ	NRZ
Amplitude / Resolution	0.3V to 1.8 V / 10 mV	1.0V to 2.5V
Accuracy HiLevel /Amplitude	±2%±10mV	±5% ±50mV
External termination voltage	-2V to +1.5V	AC Coupled
Output voltage window	-2.0 to +2.7 V	
Maximum external voltage	-2.2V to +3.3 V	
Enable / Disable	Relay	-
Transition times (20%-80%)	< 60ps	<20ps (15ps typ.)
Overshoot/ringing	10% +20mV typ.	-
Jitter	< 25ps peak-to-peak	<25ps peak to peak (20ps typ.)

*** Booster input to be driven with 1.8V amplitude from E4866A Generator**

E4867A Analyzer Module

Table 5: E4867A Timing Specifications (@ 50% of amplitude, 50 Ohm to GND)	
Data range	9.5 Gbit/s to 10.8 Gbit/s
Delay (between channels)	Can be specified as leading edge delay (start delay) in fraction of bits in each channel, fine delay can be changed with-out stopping the instrument
Start Delay Range	0 to 300 ns (not limited by period)
Fine Delay Range	±1Period (w/out stopping)
Resolution	1 ps
Accuracy	±20 ps ±50 ppm relative to the zero-delay placement.
Skew between modules of same type	50 ps typ. after deskewing at customer levels and unchanged system frequency

Table 6: E4867A Pattern and Sequencing	
Segment length resolution	256bits
Patterns:	
Memory based	up to 33,554,432
PRBS/PRWS	2^n-1, n= 7, 9, 10, 11, 15, 23, 31
Marker Density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n-1, n= 7, 9, 10, 11, 15
Errored PRBS / PRWS	2^n-1, n= 7, 9, 10, 11, 15
Extended ones or zeros	2^n-1, n= 7, 9, 10, 11, 15
User	Data editor, file import
Analyzer expected Data	
Mark Density	9/10...10/9
Max consecutive 0 or 1	20000 or 2 us
Data recovery from imbalanced	200 us
Analyzer Auto-synchronization	on PRBS or Memory based Data manual or automatic by: Bit synchronization* with or without automatic phase alignment. Automatic delay alignment around a start sample delay BER Threshold: 10^{-4} to 10^{-9}

***Bit synchronization on data is achieved by detecting a 48Bit unique word at the beginning of the segment. (Don't cares can be programmed within the detect word). In this mode memory-based data cannot be sent within the same system. If several inputs synchronize, the delay difference between the terminals must be smaller ±5 segment length resolution.**

In general every time a sequence is started this AC coupled behavior has to be taken into account. There are two different methods of dealing with it, without getting invalid results.

1. Whenever possible use the synchronization feature (Bit Sync. or Auto Delay Alignment) followed by a balanced pattern according to the specification above. In this case no recovery time is needed after starting a sequence.
2. If for some resason synchronization is impossible, use a preamble instead. The length of such a data segment will correspond to the specified settling time. The pattern of the preamble as well as the following data segment must not exceed the maximum tolerated imbalance (9/10 to 10/9).

Synchronization

Synchronization is the method of automatically adjusting the proper bit phase for data comparison on the incoming bit stream. The synchronization can be performed on PRBS/PRWS and memory-based data (it is not possible on a mix of PRxS and memory based data). There are two types of sychronization:

- Bit synchronization
- Auto delay alignment

Bit synchronization is possible to cover a bit aligment for a totally unknown number of cycles. Using memory based data, the first 48 Bit within the expected data segment will work as DETECT word where the incoming data are compared to. When the incoming data match with this Detect Word, the further analysis will be started.

Auto Delay aligment will be performed using the analyzer sampling delay. So there is a limited range while this is possible of 10 ns. Using Auto delay alignment will provide synchronization with an absolute timing relation between a group of analyzer channels. Therefore skew measurements will be possible.

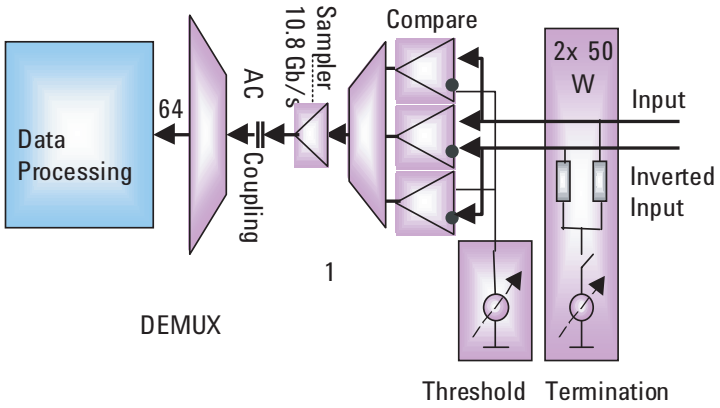


Figure 1: Internal AC Coupling of E4867A Analyzer

Input/Output

Addressable technologies:

CML, SSTL-2, ECL (terminated to 0 V/-2 V), LVPECL, (terminated to 1.3V)

Generator Out

The Generator output can be used single ended or differential. Enable/Disable relay provide on/off switching. Switched off will provide internal termination. It is recommended either to turn off or externally terminate unused outputs.

The generator outputs can work into 50 Ohm center tapped termination or 100 Ohm differential termination. The proper termination scheme can be chosen from the editor to adapt proper level programming.

Analyzer Input

The analyzer input provides more than 90% eye opening with an "ideal" input signal (10ps transition time). This is a superior performance for characterization tasks.

The analyzer channels can be operated:

- single-ended normal
- single-ended compliment
- differential

For termination there is always 50 Ohm connected to a programmable termination voltage. In differential mode there is an additional, selectable 100 Ohm differential termination. Independently of the selected termination, one can select whether the analysis of the incoming signal shall be performed on the input or on the complimentary input or true differentially.

Booster N4868A

The N4868A delivers either 1 differential channel or 2 single-ended channels. The N4868A 001 delivers either 2 differential or 4 single-ended channels. For differential operation it is recommended that the N4869A cable kit be used with phase adjustment capability for the differential path. For the N4868A -001 two cables kits would be needed if both are used as differential. The N4868A -001 can also be used 1x differential and 2x single-ended to boost the clock output of the E4866A beside the differential data.

Table 7: Parameters for Analyzer Module E4867A 10.8 Gbit/s

Inputs	1 , differential or single ended	
Impedance	50 Ohm typ. 100 Ohm differential if termination voltage is switched off	
Input sensitivity	100 mV typ.,single-ended and differential	
Internal termination voltage	-2.0 to +2.0 V, can be switched off	
Threshold voltage range	-2.0 to + 2.0 V	
Threshold resolution	1 mV	
Threshold accuracy	± 2% ±20 mV	
Maximum input voltage range three ranges selectable:	-2V to + 0V, -1V to +1V, 0V to 2V	
Maximum differential voltage	1.2V	
Enable / Disable	Relay	
Bandwidth, equivalent transition time (20%-80%)	35ps typ.	
Minimum detectable Pulse Width	Data:	80 ps typ.
	Continuous clock:	40 ps typ.
Phase Margin with ideal input signal with E4866A Generator.	>1 UI -15ps > 1 UI -33ps	

E4861B ParBERT 3.35 Gb/s Data Module
E4862B ParBERT 3.35 Gb/s Generator Front-End
E4863B ParBERT 3.35 Gb/s Analyzer Front-End
Technical Specifications

E4861B with E4862B & E4861B with E4863B

General

A ParBERT 3.35 Gbit/s module houses two front-ends, either two generators or analyzers or any mix. ParBERT 3.35 Gbit/s modules run with the E4808A module. The key specifications of ParBERT 3.35 Gbit/s are:

- 21MHz ... 3.350 GHz Clock/data rate
- 16Mbit memory depth at each channel
- HW based PRBS generation up to the polynomial of 2^{31}-1
- analyzer can synchronize on a 48bit detect word (memory based data)
- analyzer can synchronize on a pure PRBS pattern without detect word.

Timing Capabilities

The frequency range of the modules is 21MHz ... 3.350GHz. The ParBERT 3.35Gbit/s front-ends use a multiplying PLL that multiplies system master clock by 4 or 8. With the help of the clock module, an external clock source can be used. This external clock must run continuously. If the clock signal is interrupted, the multiplying PLLs typically needs 100 milliseconds to lock onto the clock again.

Sequencing

The sequencer receives instructions from the clock module. The channel sequencer can generate a sequence with up to 120 segments. The Sequencer has 2 loop levels, which allow nested loops. An analyzer channel can generate feedback signals which are combined in the Clock module for a common reaction of all parallel channels. In case of a single receive channel the channel sequencer itself can handle the feedback signals.

Table 1: E4861B Data Generator Timing Specification (@ 50% of amplitude, 50 Ohm to GND)

Frequency range	20.834 MHz to 3.350 GHz
Delay=start delay+fine delay	Can be specified as leading edge delay in fraction of bits in each channel
Start Delay Range	0 to 200ns (not limited by period)
Fine Delay Range	+/- 1 Period (can be changed without stopping)
Delay Resolution	1 ps
Accuracy Data Mode	±25 ps ±50 ppm relative to the zero-delay and temperature change within ±10°C after autocalibration
Clock mode	±50 ps ±50 ppm relative to the zero-delay
Skew between modules of same type (Data Mode)	50 ps typ. after deskewing at customer levels and unchanged system frequency

The variable delay is available in data mode and pulse mode. In clock mode the timing is fixed.

Table 2: E4861B Analyzer Timing All timing parameters are measured at ECL levels, terminated with 50 Ohm to GND

Sampling rate	Same as generator
Sample Delay	Same as Delay = start delay + fine delay
Start Delay Range	Same as generator
Fine Delay Range	Same as generator
Resolution	Same as generator
Accuracy	Same as generator
Skew	Same as generator

Table 3: E4861B Pattern and Sequencing	
Patterns:	
Memory based	Up to 16Mbit
PRBS/PRWS	
Marker Density	2^n-1, n=7, 9, 10, 11, 15, 23, 31
Errored PRBS/PRWS	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n-1, n=7, 9, 10, 11, 15
Extended ones or zeros	2^n-1, n=7, 9, 10, 11, 15
Clock patterns	2^n-1, n=7, 9, 10, 11, 15
User	Divide or multiply by 1, 2, 4
Analyzer Auto-synchronization	On PRBS or Memory-based Data Manual or automatic by: Bit synchronization* with or without automatic phase alignment around a start sample delay (Range: ±50ns) BER Threshold: 10^4 to 10^8

***With PRBS data, analyzers can autosyncronize on incoming PRBS data bits. When using memory-based data, this data must contain a unique 48 bit detect word at the beginning of the segment, and the generators must be on a separate system clock. Don't cares within detect word are possible. If several inputs synchromize, the delay difference between terminals must be smaller than ±5 segment lengths.**

Table 4:	
No. of segments	120 - no. of loops
Loop levels	2
Loop length	(2 ... 2^{20}) Mux-factor

Table 5: Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range Mbit/s	Segment length resolution	Maximum memory depth, bits
20.834 ... 41.666	1bit	131,072
20.834 ... 82.333	2bits	262,144
20.834 ... 166.666	4bits	524,288
20.834 ... 333.333	8bits	1,048,576
20.834 ... 666.666	16bits	2,097,152
20.834 ... 1,333.333	32bits	4,194,304
20.834 ... 2,700.000	64bits	8,388,608
20.834 ... 3,350.000	128bits	16,777,216

Table 6: Dependancy of PRWS generation and port width. Almost all the combinations are possible except the following:

PRWS	Port Width
2^7 -1	No restriction
2^9-1	7
2^{10}-1	3, 11, 31, 33
2^{11}-1	23
2^{15}-1	7, 31
2^{23}-1	47
2^{31}-1	No restriction

Pattern Generation

The data stream is composed of segments. A segment can be of the type memory-based pattern, memory-based PRBS or hardware generated PRBS. A total of 16Mbit (at segment length resolution 128bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to 2^{15}-1 or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio. A zero substitution pattern extends the longest zero series by a user-selectable number of additional zeros. The next bit following these zero-series will be forced to 1. Mark ratio is the ratio of ones and zeros in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4, 7/8. Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 128 the number of repetitions is also 128. That means that a 2^{15}-1 PRBS uses up to 4Mbit of the memory.

Hardware-based PRBS can be of any polynomial up to a degree of 2^{31}-1. No memory is used, so the total memory is free for memory-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. In case of an error a bit will be inverted, so instead of a '0' a '1' is generated and vice versa. Single errors can be inserted by P or via instructions from the Central sequencer. The user can trigger an error with a signal supplied to the qualifier pod of the Central module. An error insertion with a fixed rate and a fixed distribution is supported. The user software allows the selection of errored and error-free segments.

Generator Front-End (E4862B)

The amplifier generates a differential output signal. Each output can be individually switched on and off. The output levels are sufficient to drive typical high-speed devices with interfaces like ECL, LVPECL, and LVDS. The nominal output impedance is 50 Ohm. The Delay Control In has a single-ended input with 50 Ohm impedance. The input voltage modulates a Delay element within the generator's differential output. The user has the option of turning the Delay Control In feature on or off. Additionally the user can select between two delay ranges.

Table 7: Parameters for Generator Front-Ends E4862B 3.35 Gbit/s		
Outputs	1, differential or single-ended	
Impedance	50 Ohm typ.	
Data formats	Data: NRZ, DNRZ, RZ, R1	
Pulse Mode		
Range	150ps to (1UI - 150ps)	
Resolution	1ps	
Width accuracy	40 ps typ.	
Output voltage window	-2.00 to +3.00 V	
Absolute maximum external voltage	-2.2 V to +3.2 V	
Addressable technologies	LVDS, CML, PECL, ECL low voltage CMOS	
Amplitude/Resolution	0.05 Vpp ... 1.8 Vpp/10 mV	
Accuracy HiLevel/Amplitude	±2% ±10 mV	
Short circuit current	72 mA max.	
Transition times (20%-80%)	<75ps; 60ps typ.	
Overshoot/ringing	5% +10 mV typ.	
Jitter, NRZ data mode	<30ps peak-peak	**(1)**
Clock mode	<2ps rms	**(1,2)**
Pulse, RZ, R1 mode	30ps peak-peak typ.	**(1,2)**
Cross-point adjustment (Duty cycle distortion)	30% ... 70% (in NRZ mode only)	

(1) Measured with E4808A Clock Module
(2) Specified as Intra Channel Jitter.

Table 8: Delay Control In	
Input voltage window	-500mV ... +500mV (DC-coupled)
Delay Range 1	-250ps ... +250ps
Delay Range 2	-25ps ... +25ps
Modulation Bandwidth	DC ... 200MHz
Input Impedance	50 Ohm (typ.)

Analyzer Front-End (E4863B)

The analyzer features are:
- Acquire data from start
- Compare and acquire data around error
- Compare and count erroneous ones and zeros to calculate the Bit-Error-Rate Receive memory for acquired data up to 16Mbit deep, depending on the segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum granularity.

The analyzer is able to synchronize on a received data stream by means of a user-defined Detect Word. The Detect Word is defined by the first bits within the expected segment, it has a length of 48 bits and is composed of zeros, ones and Xs (don't cares). The detect word must be unique within the data stream. Synchronization on a pure-PRBS data-stream is done without a detect-word, by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ohm impedance. The sensitivity of down to 50mV and the common mode range of the comparator allows the testing of all common differential high-speed devices. The user has the option of using the differential input with or without termination voltage or as single-ended input (with termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

Table 9: Parameters for Analyzer Front-Ends E4863B 3.35 Gbit/s

Number of channels	1, differential or single-ended	
Impedance	50 Ohm typ. (100 Ohm differential if termination voltage is switched off)	
Internal termination voltage (can be switched off)	-2.0 to +3.0 V	
Threshold voltage range	-2.0 to +3.0 V	
Threshold resolution	1 mV	
Threshold accuracy	±20 mV ±1%	
Input sensitivity (single-endedand differential)	<50mV	
Minimum detectable pulse width	<150ps	
Maximum input voltage range	Three ranges selectable: -2V to +1V -1V to +2V 0V to 3V	
Maximum differential voltage	1.8V	
Phase margin with ideal input signal	>1UI - 30ps	**(1)**
Phase margin with E4862B Generator	>1UI - 50ps	**(1)**
Auxilary out	V out: 350mV pp typ., AC coupled	**(2)**

(1) Measured with E4808A Central Module
(2) Terminate with 50 Ohm to GND, if not used

Protection

Input and output relay switch off automatically, if absolute maximum voltage window is exceeded.

E4861A ParBERT 2.7 Gb/s / 1.65 Gb/s Data Module
E4862A ParBERT 2.7 Gb/s Generator Front-End
E4863A ParBERT 2.7 Gb/s Analyzer Front-End
E4864A ParBERT 1.65 Gb/s Generator Front-End
E4865A ParBERT 1.65 Gb/s Analyzer Front-End
Technical Specifications

E4861A Generator/Analyzer Module

This module holds any combination of up to two analyzer front-ends (E4863A, E4865A) and generator front-ends (E4862A, E4864A).

With front-ends E4864A and E4865A the maxiumum speed is limited to 1.65 Gbit/s. The maximum speed of 2.7 Gbit/s is achieved with front-ends E4862A and E4863A.

Clock Module/Data Mode

The generator can operate in clock mode or data mode. Clock mode is achieved when the generator is assigned as a Pulse Port. Data mode is achieved when using it as a Data Port. In clock mode there is a fixed duty cycle of 50%. In data mode there is NRZ format with variable delay. The analyzer always works as Data Port with variable sampling delay. The sampling delay consists of two elements: the start delay and the fine delay. The fine delay can be varied within ±1 period without stopping.

Data Capabilities

PRBS/PRWS and memory-based data are defined by segments. Segments are assigned to a generator for a stimulating pattern, on an analyzer it defines the expected pattern which the incoming data are compared to. The expected pattern can be set up with mask bits.

The segment length resolution is the resolution to which the length of a pattern segment or mask can be set. The maximum memory per channel of the E4861A can be set in steps of 64 bits up to a length of 8192 kbits. If the 64 bit segment length resolution is too coarse, memory depth and frequency can be traded.

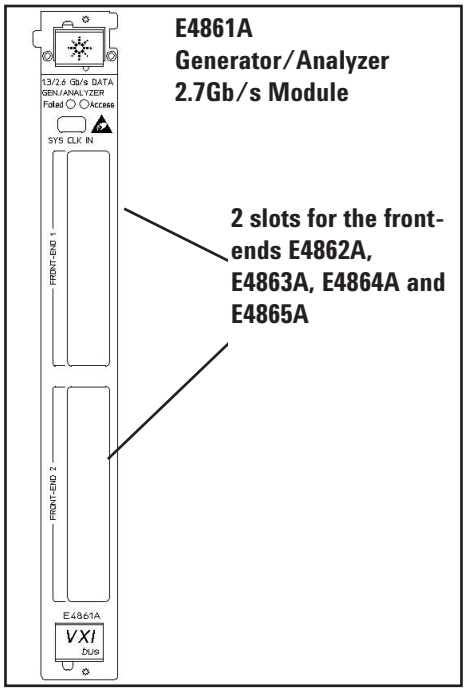


Figure 1: E4861A Module

Table 1: E4861A Data Generator Timing Specifications (@ 50 % of amplitude, 50 Ohm to GND)	
Frequency range* Clock/Data mode 333.334 Mbit/s to 2.70 Gbit/s (1.65Gbit/s E4864A, E4865A)	
Delay (between channels)	Can be specified as leading edge delay in fraction of bits in each channel
Range	0 to 300 ns (not limited by period)
Resolution	1 ps
Accuracy	±50 ps ±50 ppm relative to the zero-delay placement. (From 20°C to 35°C without autocol) ±80 ps ±50 ppm typ. relative to the zero-delay placement and temperature change within ±5°C after autocalibration
Skew between modules of same type	50 ps typ. after deskewing at customer levels and unchanged system frequency
Pulse width	50% of period typ. in clock mode

***See tables for front-end deratings**

Table 2: E4861A Analyzer Timing All timing parameters are measured at ECL and levels, terminated with 50 Ohm to GND	
Sample delay= start delay + fine delay, fine delay can be changed without stopping	
Sampling rate*	Same as generator
Fine delay range	±1 period
Sampling delay range	Same as generator
Accuracy	Same as generator
Resolution	Same as generator
Skew	Same as generator

***See tables for front-end deratings**

Table 3: E4861A Pattern and Sequencing	
Patterns:	
Memory-based	up to 8Mbit
PRBS/PRWS	2^n-1, n=7, 9, 10, 11, 15, 23, 31
Marker Density	1/8, 1/4, 1/2, 3/4, 7/8 at PRBS/PRWS 2^n-1, n=7, 9, 10, 11,15
Errored	2^n-1, n=7, 9, 10, 11, 15
Extended ones or zeros	2^n-1, n=7, 9, 10, 11, 15
Clock patterns	Divide or multiplied by 2, 4, 8, 16
User	Data editor, file import
Analyzer Auto-	On PRBS or memory-based data
Synchronization:	manual or automatic by: Bit synchronization* with or without automatic phase alignment Automatic delay alignment around start sample delay (Range: ±10ns) BER Threshold: 10^4 to 10^9

***Bit synchronization on data is achieved by detecting a 48 Bit unique word at the beginning of the segment. Don't cares within the detect word are possible. In this mode no memory-based data can be sent within the same system. If several inputs synchronize the delay difference between the terminals, it must be smaller ±5 segment length resolution.**

Table 4: Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range M/bits	Segment length resolution	Maximum memory depth, bits
333.334...666.666	16 bits	2,097,152
666.667...1,333.333	32 bits	4,194,304
1,333.334...2,666.667	64 bits	8,388,608

In general it is possible to set higher values for the segment length resolution and also at lower frequencies than are indicated in the table

Table 5: Depending on the capability of generating PRWS and port width, almost all the combinations are possible except the following:

PRWS	Port Width
2^7-1	No restriction
2^9-1	7
2^{10}-1	3, 11, 31, 33
2^{11}-1	23
2^{15}-1	7, 31
2^{23}-1	47
2^{31}-1	No restriction

Sub-frequencies

For applications requiring different frequencies at a fraction of the system clock, the rate can be divided or multiplied by 1, 2 or 4. This influences the dependency between segment length resolution and maximum memory depth.

Synchronization

Synchronization is the method of automatically adjusting the proper bit phase for data comparison on the incoming bit stream. The sychronisation can be performed on PRBS/PRWS and memory based data but it is not possible on a mix of PRxs and memory-based data.

There are two types of synchronization
- bit synchronization
- auto delay aligment

Bit synchronization is possible to cover a bit aligment for a totally unknown number of cycles. Using memory-based data, the first 48 bit within the expected data segment will work as Detect Word which the incoming data are compared to. When the incoming data match with the Detect Word, further analysis begins.

Auto Delay aligment is performed by using the analyzer sampling delay. So there is a limited range while this is possible of ±10ns.

Using Auto Delay alignment will provide synchronization with an absolute timing relation between a group of analyzer channels. So skew measurements are possible.

Table 6: Parameters for Analyzer Front-Ends E4863A 2.7 Gbit/s (E4865A 1.65 Gbit/s)	
Number of channels	1, differential or single ended
Impedance	50 Ohm typ. 100 Ohm differential if termination voltage is switched off
Internal termination voltage (can be switched off)	-2.0 to +3.0 V
Threshold voltage range	-2.0 to + 3.0 V
Threshold resolution	2 mV
Threshold accuracy	± 1% ±20 mV
Input sensitivity (single-ended and differential)	50mV typ
Minimum detectable pulse width	180 ps typ. at ECL levels
Maximum input voltage range	Three ranges selectable: -2V to + 1V -1V to +2V 0V to 3V
Maximum differential voltage	1.8V operating max. 3V
Phase Margin, with ideal input signal **with generator E4862A**	>1UI - 50 ps > 1UI-75 ps
Auxiliary out	Swing: 400 mV pp typ., AC coupled

Table 7: Parameters for Generator Front-ends E4862A 2.7 Gbit/s (E4864A 1.65 Gbit/s)	
Outputs	1, differential or single-ended
Impedance	50 Ohm Typ.
Formats	Clock: Duty cycle 50%±10% typ. Data: NRZ, DNRZ
Output voltage window	-2.00 to + 3.00 V 3.00 V to 4.5(terminated to +3V only)
Maximum external voltage	- 2.2 to +4.7 V
External termination voltage	-2V to +3V
Amplitude/Resolution	low voltage CMOS 0.05 to 1.8 Vpp*/10 mV
Accuracy HiLevel/Amplitude	±2% ±10 mV
Short circuit current	72 mA max.
Transition times (20%-80%)	90ps typ @ ECL,LVDS 110ps typ @ Vpp max
Overshooting/ringing	20% + 20mV typ
Jitter, Data mode	<50ps peak-to-peak
Clock mode	<5ps, rms

***does double into open, but outputs may switch off**

Input/Output

Addressable technologies

LVDS, ECL (terminated with 50 to 0 V/-2 V), PECL (terminated to +3 V Analyzer input requires use of a Bias Tee).

Analyzer Input

The analyzer channel can be operated:

- Single-ended normal
- Single-ended compliment
- Differential

For termination there is always 50 Ohm connected to a programmable termination voltage. In differential mode there is an additional, selectable 100 Ohm differential termination. Independent of the selected termination, there is the choice of whether the anaylsis of the incoming signal is performed on the input or true differentially. For connecting to PECL it is recommended a Bias Tee is used. The 2.7 Gb/s analyzer offers an auxiliary output, where the differential input signal is available as a single-ended signal. The bandwidth of the Aux Output is limited to 2GHz.

Generator Output

The Generator output can be used as single-ended or differential. Enable/Disable relays provide on/off switching. When switched off internal termination is provided. It is recommended that unused outputs are either turned off or externally terminated.

The Generator outputs can work into 50 Ohm centre tapped termination or 100 Ohm differential termination. The proper termination scheme can be chosen from the editor to adapt proper level programming.

Protection

Input and Output Relays switch off automatically if maximum voltages are about to be exceeded.

E4832A ParBERT 675 Mb/s Data Module
E4838A ParBERT 675 Mb/s Generator Front-End
E4835A ParBERT 675 Mb/s Analyzer Front-End
Technical Specifications

E4832A 675 Mbit/s Generator/Analyzer Module

This module holds any combination of up to two analyzer front-ends (E4835A) and four generator front-ends (E4838A),

Clock Module/Data Mode

The generator can operate in clock mode or data mode. Clock mode is achieved when the generator is assigned as a Pulse Part. Data mode is achieved with assigning it and data part. In Clock mode there is a fixed duty cycle of type 50%. In data mode there is NRZ format with variable delay. The analyzer works as data part always with variable sampling delay. The sampling delay consists of two elements: the start delay and the fine delay. The fine delay can be varied within ±1 period without stopping.

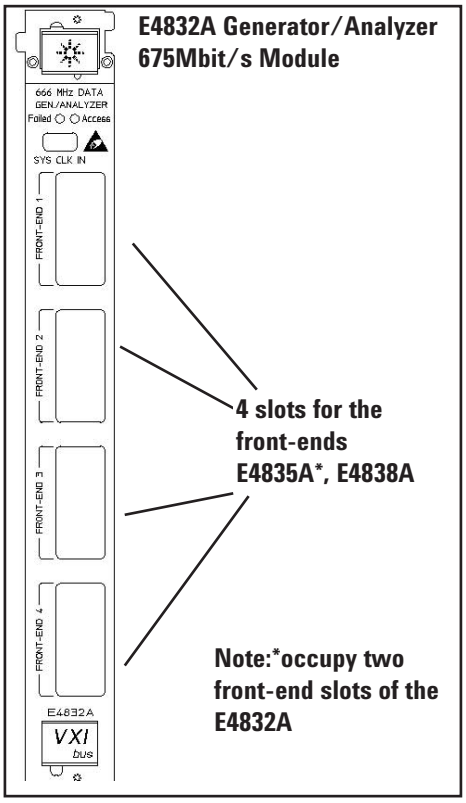
Data Capabilities

PRBS/PRWS and memory based data are defined by segments. Segements are assigned to a generator for a stimulating pattern, on an analyzer it defines the expected pattern where the incoming data are compared to. The expected pattern can be setup with mask bits.

The segment length resolution is the resolution to which the length of a pattern segment can be set. The maximum memory per channel of the E4832A can be set in steps of 16 bits up to a length of 2048 Kbit. If the 16-bit segment length resolution is too coarse, memory depth and frequency can be traded as shown in table 28.

Sub-frequencies:

For applications requiring different frequencies at a fraction of the system clock, the ratio can be divided or multiplied by 2, 4, 8, or 16. This influences the dependency between segment length resolution and maximum memory depth.



E4832A Module

Table 1: E4832A Data Generator Timing Specifications (@ 50% of amplitude, 50 Ohm to GND and fastest transition times)

Frequency range	333,334 kHz to 675 MHz
Delay range	0 to 3.0 µs (not limited by period)
Resolution	2 ps
Accuracy	±50 ps ±50 ppm relative to the zero-delay Placement*
Skew	50 ps typ. after deskewing at customer levels
Pulse width	Can be specified as width or % of duty cycle
Range	750 ps to (Period-750 ps)
Resolution	2 ps
Accuracy	±200 ps ±0.1%
Duty Cycle	1% to 99%, subject to width limits

***Valid at 15 ... 35°C room temperature**

Table 2: E4832A Analyzer Timing All timing parameters are measured at ECL and levels terminated with 50 Ohm to GND	
Sample delay=start delay+fine delay	
Fine delay can be changed without stopping**	
Sampling rate*	Same as generator
Fine delay range	±1 period
Sampling delay range	Same as generator
Accuracy	Same as generator
Resolution	Same as generator
Skew	Same as generator

***See tables for front-end deratings**
****Conditions: frequency > 20.8 MHz and by using the finest segment length resolution.**

Table 3: Pattern and Sequencing features of E4832A	
Patterns:	
Memory-based	up to 2Mbit see table 24
PRBS/PRWS	2^n-1, n=7, 9, 10, 11, 15, 23, 31
Marker Density	1/8, 1/4, 1/2, 3/4, 7/8 at PRBS/PRWS 2^n-1, n=7, 9, 10, 11,15
Errored	2^n-1, n=7, 9, 10, 11, 15
Extended ones or 0	2^n-1, n=7, 9, 10, 11, 15
Clock patterns	Divide or multiplied by 2, 4, 8, 16
User	Data editor, file import
Analyzer Auto-Synchronization:**	On PRBS or memory-based data manual or automatic by: Bit synchronization* with or without automatic phase alignment Automatic delay alignment around start sample delay (Range: ±50ns) BER Threshold: 10^4 to 10^9

***Bit synchronization on data is achieved by detecting a 48Bit unique word at the beginning of the segment. Don't cares within the detect word are possible. In this mode no memory-based data can be sent within the same system. If several inputs synchronize the delay difference between the terminals, it must be smaller ±5 segment length resolution.**
****Condition: frequency >20.8 MHz and by using the finest segment length resolution.**

Synchronization

Synchronization is the method of automatically adjusting the proper bit phase for data comparison on the incoming bit stream. The sychronization can be performed on PRBS/PRWS and memory based data but it is not possible on a mix of PRxs and memory based data.

There are two types of synchronization:
- Bit synchronization
- Auto delay alignment

Bit synchronization is possible to cover a bit alignment for a totally unknown number of cycles. Using memory-based data, the first 48 bit within the expected data segment will work as Detect Word which the incoming data are compared to. When the incoming data match with this detect word, the further analysis will be started.

Auto Delay alignment will be performed by using the analyzer sampling delay. Therefore there is a limited range of 50ns while this is possible.

Using Auto Delay alignment will provide synchronization with an absolute timing relation between a group of analyzer channels. So skew measurements are possible.

Table 4: Data rate range, segment length resolution, available memory for synchronization and fine delay operation		
Data rate range Mbit/s	**Segment length resolution**	**Maximum memory depth, bits**
20.834 ... 41.666	1bit	131,008
41.667 ... 83.333	2 bits	262,016
83.334 ... 166.666	4 bits	524,032
166.667 ... 333.333	8 bits	1,048,064
333.334 ... 666.667	16 bits	2,097,152

In general it is possible to set higher values for the segment length resolution and also at lower frequencies than is indicated in the table. In this case the fine delay function and the auto-synchronization function are unavailable.

Table 5: Depending between the capability of generating PRWS and port width. Almost all the combinations are possible except the following:	
PRWS	**Port Width**
2^7-1	No restriction
2^9-1	7
2^{10}-1	3, 11, 31, 33
2^{11}-1	23
2^{15}-1	7, 31
2^{23}-1	47
2^{31}-1	No restriction

Input/Output

Addressable technologies

LVDS, (P)ECL, TTL, 3.3 V CMOS

Analyzer Input

The analyzer channel can be operated:

- Single-ended normal
- Single-ended compliment
- Differential

For termination there is always 50 Ohm connected to a programmable termination voltage. In differential mode there is an additional, selectable 100 Ohm differential termination. Independent of the selected termination, there is the choice of whether the anaylsis of the incoming signal is performed on the input or true differentially.

Table 6: Level Parameters for Differential Generator Front-end E4838A 675 Mbit/s		
Number of channels		1, differential
Impedance		50 Ohm typ.
Data formats		RZ, R1, NRZ, DNRZ
Output voltage window		-2.2 to +4.4 V (doubles into open up to max. 5 Vpp)
Amplitude / Resolution		0.1V to 3.50 V / 10 mV
Level accuracy		±3 % ± 25 mV typ. after 5 ns settling time
@LVDS/(P)ECL		±1 % ±25 mV typ. after 5 ns settling time
Variable transition time range (10-90% of amplitude)		0.5 to 4.5 ns
Accuracy		±5% ±100 ps
@LVDS/(P)ECL (20-80% of amplitude)		0.35 ns typ
Overshoot/ringing		< 7% (< 5% typ).
Jitter	**Data mode**	<100 ps peak to peak ((80ps typ)
	Clock mode	8ps rms typ.
Channel addition		XOR and analog

Table 7: Two Differential Analyzer Front-Ends E4835A[1], 667 MSa/s	
Number of channels	2, differential or sinle ended (switchable)
Impedance	50 Ohm typ. 100 Ohm differential if termination voltage is switched off
Termination Voltage (can be switched off)	-2.0 to +3.0 V
Threshold voltage range/ Threshold accuracy	-2.00 to +4.50 V/±1% ±20mV
Threshold resolution	2 mV
Input sensitivity	Differential 50 mV typ Single-ended 100 mV typ
Minimum detectable pulsewidth	400ps typ. at ECL levels Two ranges selectable:
Input voltage range	0 to +5 V and -2 to +3 V
Phase Margin with ideal input signal	>1UI-100ps
with E4838A Generator	>1 UI-180ps

[1]occupy two front-end slots of the E4832A. The E4835A contains two front-ends (E4835AZ) and one common data back end. In this document we refer to one front-end as E4835A.

E4809A 13.5 GHz Central Clock Module
E4808A High Performance Central Clock Module
E4805B 675 MHz Central Clock Module
Technical Specifications

Each ParBERT 81250 system consists of at least one clock module, which generates the system clock for at least one generator or analyzer or any mix.
Please see the table to the right for a complete compatibility overview!

Modules/Central Clock	E4805B	E4808A	E4809A
E4832A - ParBERT 675 Mb/s	•	•	•
E4861A - ParBERT 2.7/1.6 Gb/s	•	•	
E4861B - ParBERT 3.35 Gb/s		•	•
E4810A/11A - ParBERT 3.3.5 Gb/s optical		•	•
E4866A/67A - ParBERT 10.8 Gb/s		•	
N4872A/73A - ParBERT 13.5 Gb/s			•
E4868B/69B - ParBERT 45 Gb/s		•	

Sequencing
The sequencing can be used to specify the data flow:
- single
- looped
- infinitely
- event handling (branch)
- synchronization.

Event Handling
With the event handling the flow of data generation and Analysis can be influenced with external signals at run time.
Usage of Events:
- stop and go of data
- match loop
- intergration with other equipment (ATE)
- trigger on error

Master slave, multi-mainframe, different clock groups.
Up to 3 clock modules can be combined to run in one clock grouping by connecting the master slave cable. This is used to combine channels which do not fit into one frame into one clock group. Omitting the master-slave connection will run the channels within separated clock groups. A system can be operated using different clock groups. So a bunch of channels are combined with a clock module. The frequencies used can be totally asynchronous or m/n ratio (see clock input multiplier/divider). For separated clock groups the master slave must not be connected. Within one system the modules must always be of the same type.

E4809A, E4808A and E4805B Sequencing Features	
Number of Segments	1 to 30 (every segment looped once) 1 to 60 (no segment looped)
Looping levels	Up to 4 nested loops plus one optional infinite loop Loops can be set independently from 1 to 2 repetitions
Start/stop	External input, manual, programmed (stop with E4832A only)
Event handling	React on internal and external events. Details see next table

E4809A, E4808A and E4805B Event Handling
Event trigger sources
Events can be defined as any combination of the following sources. A maximum of 10 events can be defined.
- 8-line trigger input pod for TTL signals
- VXI trigger lines TO and T1
- Any capture error/or no error detected by one of the analyzer channels
- Software command control: an event trigger command issued locally or remotely
Reactions to an event can be set per data segment immediately or deferred and can be any combination of:
- Data segment jump
- Launch trigger pulse to the trigger output of the Clock Module
- VXI trigger lines TO and T1 can be set to 01, 10 or 11

E4809A, E4808A and E4805B Trigger Pod characteristics		
Input Lines	8, single-ended	
Input levels	TTL compatible	
Input threshold	1.5 V	
Input termination	5 k Ohm pullup to +5 V	
Absolute max. ratings for input voltages	-1.2 V to + 7.0 V	
Cable delay	11 ns typical	
sampling clock frequency	system frequency/segment length resolution	
	TRIGGER OUTPUT	CLOCK/REF INPUT
Setup time*	2.5ns	-12.5ns
Hold time *	5 ns	20 ns

***includes the cable delay**

E4809A 13.5 GHz Central Clock Module

General:
E4809A is a 2-slot central clock module enhancing the capabilities of the E4808A by a 13GHz clock distribution. ParBERT 81250 13.5 Gb/s modules are designed to run with the E4809A 13.5 GHz Central Clock module.

Timing Capabilities

The E4809A supports three different operation modes.

- **E4809A as system clock**

The E4809A distributes clock signals to connected modules in the range from 20.834 MHz up to 13.5 GHz. The E4809A provides GigaClock signals in a range from 500 MHz up to 13.5 GHz to the ParBERT 81250 13.5 Gb/s modules (N4872A, N4873A). All other supported modules are working with the E4809A MasterClock.

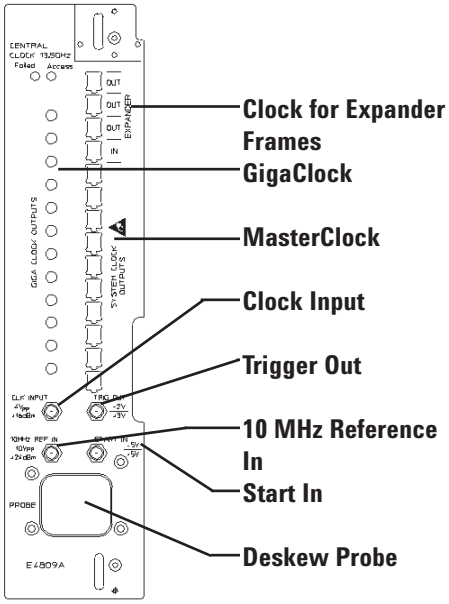
- **External Clock mode**

The system will run synchronously to an external clock, which is connected to the clock module's clock input. There are two different sub-modes available.
In the **direct** clock mode, the PLL (Phase Locked Loop) is bypassed and an external clock signal can be distributed to all GigaClock connected modules. This direct external clock mode is operating in a range from 500 MHz to 13.5 GHz. In this mode the external clock may be FM or PM modulated.
In the **indirect** external clock mode, the clock modules internal PLL is used to generate flexible MasterClock and GigaClock signals.

- **Clock Data Recovery (CDR) mode**

If the CDR is used, the CDR Out of the Analyzer must be connected to the Clock Input of the Clock module.

E4809A Clock Module specifications		
Frequency range	20.834MHz...13,5GHz	
Resolution	1Hz	
SSB Phase Noise (at 10kHz offset)	<-75dBc at 10GHz	
Latency (typical)	To Trigger output	to channel output
External Start	16ns +/-1clock	tbd ns +/- 1clock
	Add 3ns if an expander frame is used	



E4809A

Start Input

A data sequence generation can be started by an external signal.

Start Input	
Start Input	DC coupled; 3.5mm(f)
Threshold range	-1.40V to +3,70V
Zin/Termination voltage	50 Ohm typ. / -2V to +3V
Sensitivity/max. levels	200mVpp / -3V...+6V

Reference Input

The Reference Input allows ParBERT to run synchronously with an external 10MHz clock. Usage of a continuous clock is necessary. Burst clock cannot be used as an external clock.

Reference Input	
Reference Input	AC coupled; 3.5mm(f)
Frequency	10MHz
Input transition/slope	<20ns
Required Duty cycle	50+/-10%
Zin	50 Ohm
Sensitivity	200mVpp

Clock Input

This input runs ParBERT synchronously with an external clock. Usage of a continuous clock is necessary. Burst clock can not be used as an external clock. Two modes are selectable: Indirect external clock mode (clock module PLL is used) and Direct external clock mode (clock module is bypassed).

Clock Input	
Clock Input	AC coupled; 3.5mm(f)
Frequency range	
Indirect mode	20.834MHz...13.5GHz
Direct mode	500MHz...13.5GHz
Clock Input (Indirect mode only)	m=1...256; n=1...256
Multiplier(m)/divider(n)	m*n<=1024; m/n*input frequency must fit data range input frequency/n>=1,3MHz
Input transition/slope	30 ps typ.
Zin	50 Ohm
Sensitivity	<150mV

Trigger Output

This output will be used to deliver a trigger signal to a DUT, a Digital Communication Analyzer (Agilent 86100B Series) or as a stimulus for the Analyzer deskew.

Trigger Output	
Trigger Output	DC coupled, SMP (f)
Frequency	Tbd
Output transition/slope	70 ps typ. 10/90
Zout/Termination voltage	50 Ohm / -2 to +3V
Output voltage window	-2V to +3V
Output level	0.1 to 1.8 Vpp

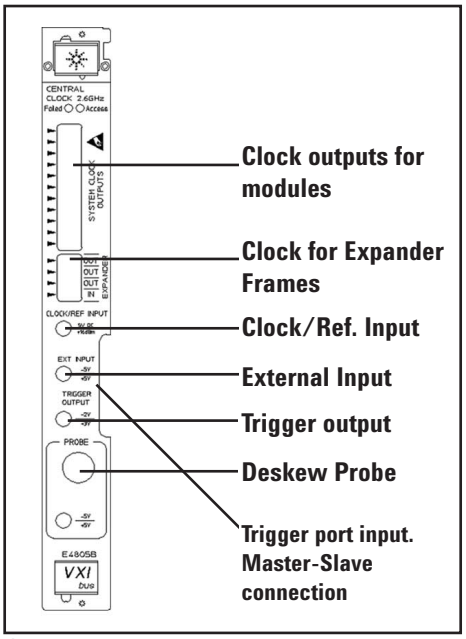
E4805B and E4808A Central Clock Modules

The central clock module includes a PLL (Phase-Locked Loop) frequency generator to provide a system clock. Depending on the frequency chosen, the data modules can be clocked at a ratio of 1, 2, 4, 8, 16, 32, 64 or 256 times higher or lower than the system clock.

External start/stop: The data running can be started by an external signal applied to the external input. With module E4832A there is also Stop and Gate mode.

Ext. Clock/Ext. Reference: This input runs ParBERT 81250 synchronously with an ext. clock, or when a more accurate reference is needed than the internal oscillator. Usage of a continuous clock is necessary. Burst clock cannot be used as an external clock. Maximum external clock is 2.7 GHz for the E4805B and 10.8Gbit/s for the E4808A. (Note: no improvement of jitter specifications will be achieved).

Guided deskew: Individual semi-automatic deskew per channel. The deskew probe 15447A allows deskew on the DUT's (Device Under Test) fixture.



Clock Module

E4805B and E4808A Clock Module specifications

	E4805B	E4808A
Frequency range*	1kHZ to 675 MHZ	170 kHz to 675 MHz
(can be entered as period or frequency)	E4805B will run with:	E4808A will run with: - E4866A/E4867A in range of 9.5GHz to 10.8GHz
E4808A Clock Module specifications	- E4861A in range of 334 MHz to 2.7GHz - E4832A in range of 334KHZ to 675 MHz	- E4861B in range of 20.834 MHz to 3.35GHz- E4861A in range of 334 MHz to 2.7GHz - E4832A in range of 334KHZ to 675 MHz
Resolution	1 Hz	1 Hz
Accuracy	±50 ppm with internal PLL reference	±50 ppm with internal PLL reference

May be limited or enhanced by modules or frontends

External input and ext. clock/ext. ref. input	E4805B		E4808A	
Zin/Termination voltage	50 Ohm/-2.10 V to 3.30 V		50 Ohm /-2.10 V to 3.30 V	
Sensitivity/max levels	400 mVpp /-3 V to + 6 V		200 mVpp /-3 V to + 6V for < 9.5Gbit/s 300mVpp/-3V to+ 6V for > 9.5 Gbit/s	
Coupling **Ext. Input:**	dc, Threshold Range: -1.40 V to +3.70 V		dc, -1.40 V to +3.70 V	
Ext. Clock/Ext. Ref:	ac		ac	
Input transitions/slope	< 20ns. Ext. input active edge is selectable		< 20 ns. Ext. Input active edge is selectable	
Clock input multiplier(m)/ divider (n)	m=1...256; n=1...256 m*n<=1024 m/n * input frequency must fit data range input frequency/n>=1.3 MHZ			
PLL lock time	100ms		100 ms	
Input frequency/period **Ext. Clock**	170 kHz - 2.7 GHz		170 kHz - 10.8 GHz	
Ext. Ref	1*, 2*, 5, or 10 MHz		1*, 2*, 5, or 10 MHz	
Required duty cycle	50 ±10 %		50 ±10 %	
Latency (typical):	to trigger Output	to channel output	to trigger Output	to channel Output
Ext. input	16ns ±1 clock	46ns ±1 clock	16ns ±1 clock	46ns ±1 clock**
Ext. clock	15ns	45ns	15ns	45ns
	Add 3ns if an expander frame is used		Add 3 ns if an expander frame is used	

*** Jitter performance may be degraded**

**** If frequency=667MHz**

Trigger Ouput

Can be used in:

- clock mode
- sequence mode

In sequence mode a pulse will be set to mark the start of any segment

The trigger output runs to a maximum 675MHZ. If a higher speed performance clock is needed;

- A 2.7GHZ Clock can be obtained from a 2.7Gb/s channel operated as a pulse port.
- A 10.8GHZ clock is available from the 10.8 Gb/s generated module as clock output.

Trigger output characteristics E4805B and E4808A	
Trigger output signals	- Clock mode (up to 675 MHz). - Sequence Mode
Output impedance	50 Ohm typ.
Output level	TTL (frequency < 180 MHz), 50 Ohm to GND ECL 50 Ohm to GND/-2 V, PECL 50 Ohm +3V
Trigger advance	30 ns typ. between trigger output and data output/sampling point (delay set to zero in both cases)
Maximum ext voltage	-2 V to +3.3 V
Jitter (int. reference/int. clock)	< 10 ps rms (5ps typ.)

General Characteristics

Mainframes: See table 34.

Save/recall: Pattern segments, settings and complete settings plus segments can be saved and recalled. The number of settings that can be stored is limited only by internal disk space.

Vector import/export: Pattern files can be imported/exported via a 3.5 inch floppy disk, LAN or GP-IB (IEEE 488.2). File format is ASCII using a STIL subset.

Programming interface: GP-IB (IEEE 488.2) and LAN. The interface to applications such as C, Visual Basic, or VEE must be installed. Agilent 81200 Plug & Play drivers for easy programming are available.

Programming language: SCPI 1992.0

Programming times: Vector transfer from memory to hardware depends on the amount of data.

On-line help: Context-sensitive.

Print-on-demand: Getting started and programming guides can be printed from .pdf files included in the ParBERT 81250 software.

Self-test: Module and system self-tests can be initiated.

Modules

Module size: VXI C-size, 1 slot.

Module type: Register-based; requires ParBERT 81250 user software E4875A supplied with the mainframes.

Weight: (including front-ends) Net: 2kg.

Shipping: 2.5 kg.

Warranty: 3 years return for repair service, depending on support option.

Re-calibration period: 1 year.

Agilent Technologies Quality Standards
The ParBERT 81250 is produced to the ISO 9001 international quality system standard as part of Agilent Technologies' commitment to continually increasing customer satisfaction through improved quality control.

Table 41: Programming Times

	Programming time
Change of levels	6 ms typ.
Change of delay	16 ms. typ. Not applicable in run mode.
Change of period	60 ms typ. For one E4805B with one E4832A. Not applicable in run mode. Increases with the number of modules but less than proportional.
Stop + start	32 ms typ.
Synchronization*	50ms typ. (without phase alignment) 110ms typ. with 20% phase accuracy @ 660MHz 650ms typ. with 1% phase accuracy @ 660MHz
Download values:	
System with 4 channels, 100,000 bit each	< 1.5 s typ.
System with 120 channels, 1 Mbit each	< 30 s typ.
System with 40 channels, 1 Mbit each	< 10 s typ.

*Add numbers for each synchronizing analyzer within one module

Table 42: Power Requirements of Modules and Front-Ends

	DC Volts	+24V	+12V	+5V	-2V	-5.2V	-12V
Modules (These specifications are valid for the module with the front-ends installed)							
E4805B Central Clock module	DC Current	0.15A	0.2A	1.8A	1.4A	3.8A	0.2A
	Dynamic current	0.0015A	0.02A	0.18A	0.14A	0.38A	0.02A
E4808A	DC Current	.35A	0.2A.	3.0A	1.2A	3.6A	0.2A
	Dynamic current	0.04 A	0.02A	0.30 A	0.12A	0.36A	0.02A
E4867A	DC Current	0.2A	1.0A	7.0A	1.5A	3.0A	0.8A
	Dynamic current	0.02A	0.1A	0.7A	0.15A	0.3A	0.08A
E4866A	DC Current	0.2A	1.0A	5.0A	1.2A	2.6A	0.5A
	Dynamic Current	0.02A	0.1A	0.5A	0.12A	0.26A	0.05A
E4861A 2.7 Gbit/s Gen./An.Module	DC Current	0.10	0.50A	5.20A	1.80A	4.00A	0.90A
	Dynamic current	0.01A	0.05A	0.52A	0.18A	0.40A	0.09A
Remark: The power requirements of E4861A include the power requirements of any two front ends							
E4861B	DC Current	0.02A	0.02A	1,8A	0,33A	0,04A	0,A
	Dynamic current	0,01A	0,01A	0,2A	0,03A	0,05A	0,A
E4832A 675 Mbit/s Gen./An. Module	DC Current	0.10A	0.10A	2.60A	0.60A	3.60A	0.10A
	Dynamic Current	0.01A	0.001A	0.26A	0.06A	0.36A	0.01A
Remark: For the module E4832A, the power specifications of the chosen front-ends (E4835A, E4838A or E4843A) have to be added to the power specifications of the E4832A module to get the overall value of the power specifications							
Front-ends							
E4835A two differential Analyzer 675 Mbit/s (E4835AZ)	DC Current		0.2A	1.2A	0.2A	0.3 A	0.3A
	Dynamic Current		0.02A	0.12A	0.02A	0.03A	0.03A
E4838A Differential Generator 675 Mbit/s MHz,var. Slopes	DC Current		0.45A	0.18A	0.07A	0.38A	0.41A
	Dynamic Current		0.045A	0.006A	0.007A	0.038A	0.041A
E4862B Generator	DC Current	0,2A	0,2A	0,7A	0,2A	0,5A	0,21A
	Dynamic Current	0.02A	0,02A	0,07A	0,02A	0,05A	0,02A
E4863B Analyzer	DC Current	0,2A	0,2A	1,8A	0,2A	0,5A	0,21A
	Dynamic Current	0,02A	0,02A	0,2A	0,02A	0,05A	0,02A

Table 43: Cooling requirements for modules with front-ends installed

Modules	ΔP mm H_2O 10°C rise	Air Flow Liter/s
E4805B	0.25	3.6
E4808A	0.25	3.6
E4832A	0.30	4.7
E4861A	0.40	5.2
E4861B*	0.40*	6.6
E4866A	0.30	5.2
E4867A	0.30*	5.5

* 15°C rise

Operating temperature	10 °C to 40 °C
Storage temperature	-20°C to +60°C
Humidity	80% rel. humidity at 40 °C
Power requirements	90-264 Vac, ± 10%, 47-66 Hz , 90-264 Vac, ± 10%, 300-440 Hz (not recommended leakage current may exceed safety limits @ > 132 Vac)
Power available for modules	950 W for 90-110 Vac supplies 1000 W for 110-264 Vac supplies
Electromagnetic compatibility	EN 55011/CISPR 11 group 1, class A + 26 dB
Acoustic noise	48 (56) dBA sound pressure at low (high) fan speed
Safety	IEC 348, UL1244, CSA 22.2 #231, CE-mark
Physical dimensions	W: 424.5 mm, 16.71 inches H: 352 mm, 13.85 inches D: 631 mm, 24.84 inches
Weight (Net)	26.8 kg 25.3 kg
Weight (shipping)(max.)	72 kg 67 kg

Short Ordering Guide - Overview

The ParBERT 81250 is a modular instrument, which can be tailored to your specific needs. There are Generator and Analyzer channels at different speed classes. The ParBERT 81250 channels consist of data modules and front-ends. The 13.5 Gbit/s, 10.8 Gbit/s and 3.35 Gbit/s are dedicated data modules for Generators and Analyzers. At 3.35 Gbit/s and 2.7 Gbit/s the data module houses 2 Front-ends, at 675 Mbit/s the data module houses 4 Front-ends. The data modules operate with help of a clock module. The combination of data modules with a clock module is called 'Clock Group' and is represented in the ParBERT 81250 Software within one User Interface. The following table lists the combination of data modules and front-ends together with usable clock modules:

	Generator	Analyzer	Clock Module	
13.5 Gbit/s	N4872	N4873	E4809A	Dedicated modules
10 Gbit/s Data module	E4866A	E4867A	E4808A	Dedicated Modules
3.35 Gbit/s Front-ends Data Module	E4862B E4861B	E4863B E4861B	E4808A or E4809A	Front-ends Data Module houses 2 Front-ends
2.7 Gbit/s/1.65 Gbit/s Front-ends Data Module	E4862A/E4864A E4861A	E4863A/E4865A E4861A	E4805B or E4808A	Front-ends Data Module houses 2 Front-ends
675 Mbit/s Front-ends Data Module	E4835A E4832A	E4835A E4832A	E4805B or E4808A or E4809A	Front-ends E4835A provides a pair of analyzers Data Module houses 4 Front-ends

The 675 Mbit/s Analyzer E4835A always comes as a pair and need to be configured side by side, providing two fully independent analyzer channels.

Entry System:

The VXI frame offers 13 slots. Besides data modules and clock modules, there is the need for a computer interface. The ParBERT 81250 works with an IEEE 1394 FireWire interface, which works with an external PC (81250 #013, #014) or a laptop (81250 #015). The IEEE 1394 FireWire card consumes one VXI slot.

Assuming the use of the Firewire interface (embedded controller) and one
Clock module in place, the Entry System can hold up to 11 (10) data modules which is equivalent to:
- 10 channels at 13.5 Gbit/s
- 11 channels at 10.8 Gbit/s and 3.35 Gbit/s optical
- 22 channels at 3.35Gbit/s or 2.7Gbit/s
- 44 channels at 675 Mbit/s.

In some circumstances these maximum numbers cannot be achieved due to power restrictions. Before finalizing a configuration, it is necessary to calculate the power budget.

Max # of channels	675 Mbits	3.35 Gbit/s or 2.7 Gbit/s or 1.65 Gbit/s	10.8 Gbit/s	13.5 Gbit/s
FireWire				
1 Frame	44	22	11	10
2 Frames	88	44	22	20
3 Frames	132	66	33	30
4 Frames	176	88	44	40

In some circumstances these maximum numbers cannot be achieved due to power restrictions.
Before finalizing a configuration, it is necessary to calculate the power budget.
More than 3 frames require more than one clock group.

Multi-Mainframe/Master-Slave:

If more channels are needed, it is possible to add expander frames. To add channels within one Clock Group, there is the limit of a maximum of two expander frames. If data modules are housed in an expander frame they need an additional clock module, this clock module must be connected to the clock module in the entry frame (master frame) with the help of the master-slave connection. This connection cares for clock and data flow synchronization between the frames. The Master-Slave connection Hardware is delivered with the expander frames. Master-Slave connection is only possible between Clock Modules of same type.

Aside from the Master-Slave Connection between the Clock modules, the controller interface also needs an extension into the expander frames:
• The FireWire interface, consuming one slot, can be “daisy-chained” from frame to frame. This would allow the configuration of a ParBERT 81250 system with virtually an unlimited number of channels (within different clock groups, see above limitation of max. channels per clock group).

Different Clock Groups

A clock group consists of a clock module, one or more data modules and the graphical user interface allowing to set the parameters. Within one clock group there can be data modules with generators and analyzer front-ends from different speed classes combined as long as with help of the binary frequency multipliers (..., 1/16, 1/8, 1/4, 1/2, 1 , 2 ,4 ,8 , 16, ...) the data rate range possible for each data module can be achieved. The configuration of more than one clock group is possible. This will combine a clock module with one or more data modules. Several clock groups may be housed in one frame or with help of expander frames. Each clock group will be operated from its own graphical user interface. The user interface will actually be assigned to a certain hardware set. If there is more than one clock group, the user interfaces may run from separate PCs, connected via LAN.
To configure more than one clock group it is recommended:
• to run different speeds (non binary ratio) between generators and/or analyzers
• to run independent phase ratio between generators and/or analyzers
• to make flexible use of data rate range when combining different speed classes
• to use custom (memory) based data and use of bit synchronization for the analyzer(s).

Using different clock groups reduces the maximum number of channels given in the previous table. Within one system using different clock groups, all clock modules must be of same type.
A Master-Slave connection must not be installed between the clock modules if different clock groups are desired.

Order Information Entry System:

1 x 81250A	System Reference
1 x 81250 # 149	Mainframe
1 x E4805B/E4808A/ E4809A	1st Clock Module

Add data modules/front ends

Decide on Controller:

1 x 81250A #013	FireWire (IEEE 1394) OC Link to VXI
1 x 81250A #014	ext. PC

or

1 x 81250A #015	Laptop including PCMCIA IEEE 1394 card

Decide on Controller Accessories:

1 x 15444A	Monitor
1 x 15445A	ext. CD-ROM

Order Information Multi Mainframe:

1 x 81250 #152	FireWire (IEEE 1394) Expamder Frame
1 x E4805B/E4808A/ E4809A	Clock Module

Add data modules/front-ends

Order Information Master-Slave/Different Clock Groups:

E4805B: clock module (usable with 675Mbit/s and 2.7 Gbit/s module)
E4808A: clock module (usable with 675 Mbit/s, 1.65 Gbit/s, 2.7 Gbit/s, 3.35 Gbit/s, 10.8 Gbit/s and 45 Gbit/s modules)
E4809A: clock module (usable with 675 Mbit/s, 3.35 Gbit/s and 13.5 Gbit/s modules)

Specific Rules: Do not mix E4809A, E4808A and E4805B:
- Master-Slave Slave connection is possible only between Clock Modules of the same type
- One system must be configured with one type of clock module

Table 46: Cable Kit Accessories

P/N	Cable Kit Description	No. of Cables	Connectors	to be used with	Bandwidth	Matching	Length	add. Parts included
15441A	SMA to SCI	10	SMA (m) - SCI (f)	675 Mbit/s	tt>= 500ps	no	1.5 m	4 SCI adapters
15442A	SMA	4	SMA (m) - SMA (m)	675 Mbit/s/ 2.7/(3.35*) Gbit/s	tt>= 100ps	no	1 m	-
15443	SMA Matched Pair	2	SMA (m) - SMA (m)	675 Mbit/s/ 2.7/(3.35*) Gbit/s	tt>= 100ps	yes	1 m	-
N4869A	SMA & Phase Shifter	3	SMA (m) - SMA (m)	E4866A Out to N4868A In	tt>= 50ps	adjustable	0.4 m	mech. Phase Shifter +-50ps
N4870A	1.85 mm Matched	2	1.85/2.4 mm - 1.85/2.4 mm	N4868A Out E4868A/B Out E4869A/B In	tt>= 15ps	+/- 1.5 ps	0.63 m	-
N4871A	SMA Matched	2	SMA (m) - SMA (m)	3.35/10.8 Gbit/s front-ends	tt>= 50ps	+/- 1.5 ps	1 m	-

***use with 3.35 Gbit/s Front-ends limits signal performance**

Product Structure - ParBERT 81250 for Oracle

Valid from 12th June 2002

P/N	Option	Description
81250A		ParBERT 81250
	#013	IEEE 1394 PC link to VXI
	#014	External PC
	#015	Laptop including PCMCIA IEEE 1394 card
	#020	Rack
	#149	Mainframe
	#150	MXI 1st Expander Frame
	#151	MXI 2nd Expander Frame
	#152	IEEE 1394 'Firewire' Expander Frame
	#0B0	Do not include Tutorial CD Rom
	#AX4	Rack flange kit

Warranty & Services

All modules automatically have 3 years Return to Agilent warranty (if bought as separate pieces).
All bundles (81250A, E4894A/95A/94B/95B/96A/97A) have 1 year on-site warranty.
An on-site repair contract or Return to Agilent contract can be purchased once the 1 year on-site warranty has expired.
Additional on-site warranty can be chosen for 3 or 5 years.
On-site productivity assistance is included in the bundles.
Standard compliant and commercial calibration can be chosen for 3 or 5 years.
Commercial calibration is NOT automatically included.

Software

E4875A		One licence and software CD ROM for ParBERT 81250

Clock Modules

E4805B		675 MHz Central Clock Module
	#UK6	Commercial cal. certificate w/ test data
E4808A		High Performance Central Clock Module
	#UK6	Commercial cal. certificate w/ test data
E4809A		13.5 GHz Central Clock Module
	#UK6	Commercial cal. certificate w/ test data

Data Modules & Front Ends

E4832A		675 Mbit/s Gen./An. Module
	#UK6	Commercial cal. certificate w/ test data
E4861A		2.7 Gbit/s Gen./An. Module
	#UK6	Commercial cal. certificate w/ test data
E4861B		3.35 Gbit/s Gen./An. Module
	#UK6	Commercial cal. certificate w/ test data
E4835A		Two Differential Analyzer Front-Ends, 675 Mbit/s
E4838A		Differential Generator Front-End, 675 Mbit/s
E4862A		Generator Front-End 2.7 Gbit/s
	#UK6	Commercial cal. certificate w/ test data
E4862B		Generator Front-End 3.35 Gbit/s
	#UK6	Commercial cal. certificate w/ test data
E4863A		Analyzer Front-End 2.7 Gbit/s
	#UK6	Commercial cal. certificate w/ test data
E4863B		Analyzer Front-End 3.35 Gbit/s
	#UK6	Commercial cal. certificate w/ test data
E4864A		Generator Front-End 1.65 Gbit/s
	#UK6	Commercial cal. certificate w/ test data
E4865A		Analyzer Front-End 1.65 Gbit/s
	#UK6	Commercial cal. certificate w/ test data
E4810A	#001	3.35 Gbit/s 850nm Electrical/Optical Generator Module
	#UK6	Commercial cal. certificate w/ test data
E4811A	#001	3.35 Gbit/s 750-1610nm Optical/Electrical Analyzer Module (calibrated @ 850 nm?
	#UK6	Commercial cal. certificate w/ test data
E4866A		Generator Module 10.8 Gbit/s
	#UK6	Commercial cal. certificate w/ test data
N4868A		10Gbit/s Booster Module (1 diff. or 2 single ended ch.)
	#UK6	Commercial cal. certificate w/ test data
	#001	10Gbit/s Booster Module (2 diff. or 4 single ended ch.)
	#U01	Commercial cal. certificate w/ test data for N4868A-001
E4867A		Analyzer Module 10.8 Gbit/s
	#UK6	Commercial cal. certificate w/ test data
N4872A		Generator Module 13.5 Gbit/s
	#UK6	Commercial cal. certificate w/ test data
N4873A		Analyzer Module 13.5 Gbit/s
	#UK6	Commercial cal. certificate w/ test data
E4868B		45/43.2Gbit/s Multiplexer Module
	#UK6	Commercial cal. certificate w/ test data
E4869B		45/43.2Gbit/s Demultiplexer Module
	#UK6	Commercial cal. certificate w/ test data

43G Bundles

E4894B		43.2 Gbit/s Pattern Generator Bundle
	#001	10.8G Analyzer Add-On Bundle
	#002	10.8G Generator & Analyzer Add-On Bundle
	UK6	Commercial cal. certificate w/ test data
E4895B		43.2 Gbit/s Error Detector Bundle
	#001	10.8Gbit/s Generator Add-On Bundle
	UK6	Commercial cal. certificate w/ test data
E4896A		45Gbit/s & 3.35Gbit/s Pattern Generator Bundle
	#001	10.8Gbit/s Analyzer Add-On Bundle
	#002	10.8Gbit/s Generator & Analyzer Add-On Bundle
	#003	Add one extra 3.35Gbit/s Generator
	#004	Add two extra 3.35Gbit/s Generators
	#005	Add one extra 3.35Gbit/s Analyzer
	#006	Add two extra 3.35Gbit/s Analyzers
	#153	Expander frame for Agilent 81250
	#UK6	Commercial cal. certificate w/ test data
E4897A		45Gbit/s & 3.35Gbit/s Error Detector Bundle
	#001	10.8G Generator Add-On Bundle
	UK6	Commercial cal. certificate w/ test data

Accessories

15440A	Adapter kit: 4* SMA (M) I/O adapters
15441A	Cable kit: 10*SMA (m) to SCI connector
15442A	Cable kit: 4*SMA (m) to SMA (m)
15443A	Matched cable pair
15444A	Monitor
15445A	External CD-ROM
15446A	8-line trigger input pod
15447A	Deskew Probe
E4839A	Test fixture
15448A	Pogo cable kit: 4*SMA(m) & 2 Pogo adapter
15449A	DUT board 50 Ohm impedance
N4869A	Cable Kit:3 cables with phase adjuster for connecting E4866A with N4868A
N4870A	Cable Kit: 2.4mm for N4868A output
N4871A	Cable Kit: SMA matched pair,50ps
N4910A	Cable Kit: matched cable pair for 13.5G

Related Literature	Pub. Number
Need to Test BER?, Brochure	5968-9250E
Agilent ParBERT 81250, Mux/Demux Application, Application Note	5968-9695E
Agilent ParBERT 81250 Parallel Bit Error Ratio Tester, Photo Card	5980-0830E
Agilent Productivity Assistance	5980-2160E
Agilent ParBERT 81250 43.2G Product Overview	5988-3020EN
Agilent 81250 ParBERT Product Note (The influence of Generator Transition times on Characterization Measurements)	5988-5948EN
Agilent ParBERT 81250 Automatic Phase Margin Measurements at 43.2 Gbit/s	5988-5654EN
Agilent ParBERT 81250 measuring a real 43.2Gbit/s eye pattern, Product Note	5988-6625en
10GbE Technology and device Characterization Product note	*5988-6960en*

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Printed in Germany March 21st 2003
5968-9188E

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